PARALLEL INVERTER AND CONVERTER OPERATION AND IMPROVEMENTS IN TRANSFORMERS

CONTRACT NO. NAS 3-2792

Third Quarterly Report For The Period
December 28, 1963 To March 27, 1964

PREPARED FOR THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

BY:
G. W. Ernsberger
H. R. Howell
A. R. Baker

Westinghouse Electric Corporation
AEROSPACE ELECTRICAL DIVISION
LIMA, OHIO

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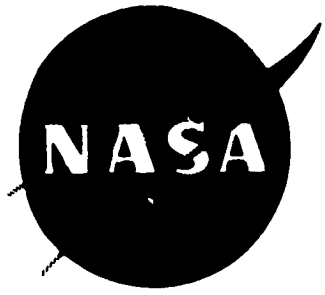

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Technical Management, NASA-Lewis Research Center
Auxiliary Power Generation Office, Francis Gourash

Westinghouse Electric Corporation
AEROSPACE ELECTRICAL DIVISION
LIMA, OHIO

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SUMMARY

The objectives of the first three quarters of this contract were (1) to improve inverter transformer weight and efficiency through the application of field-annealed doubly-oriented silicon-steel, and (2) to improve inverter and converter reliability and power capability through the development of means for parallel operation of static inverters and converters. These objectives have been met and verified through the testing and evaluation of two transformer models and the successful paralleling of two 750-watt static inverter and converter models.

The 0.006" thick doubly-oriented silicon-steel (CUBEX) used in one static-inverter output-transformer had 33% lower core loss at 13 KG flux-density than the 0.011" thick singly-oriented silicon-steel (Hipersil) used in the second transformer model. With the same amount of steel in both transformers, the static-inverter full-load efficiency increased approximately 2% when operated with the CUBEX steel transformer core.

Using the methods developed in this program, both real and reactive loads were satisfactorily shared during the static inverter paralleling evaluation. Any reasonable load division accuracy can be met and any number of static inverters or converters can be operated in parallel with the methods described.

Author

This contract has been extended for five more months to design, develop, and evaluate circuits for the automatic paralleling and protection of parallel static inverter and converter systems.

I. INTRODUCTION

The objectives of this contract were: (Task I) to evaluate field-annealing doubly-oriented silicon-steel as a means to increase the efficiency and/or the power-to-weight ratio of static inverters and converters and (Task II) to develop means to parallel static inverters and converters.

The analytical and design work for circuits to accomplish manually controlled paralleling of static inverters and converters was completed during the first quarter of the contract period. The inverter output transformer was designed with both Hipersil steel and CUBEX steel cores to compare the two magnetic materials. These accomplishments are described in the first quarterly report.

The test program used to evaluate the paralleling circuits and the transformer cores was written during the second quarter of the contract period. This test program is Appendix II of the second quarterly report and Appendix I of this report.

Fabrication of the inverter-converter test models was completed in the middle of the third quarter of the contract period. One of the test models is shown in Figure 1. The capital letters designate important component and circuit locations on the test model. Those designated are: (A) terminal boards which permit operation of the test models as either a static converter or as a static inverter (Figures 73 through 76 indicate the external connections that are necessary for either type of operation); (B) one of the quadratic transformers used in Task I of the contract; (C) the heat sink on which the power inversion stage components are mounted; (D) the countdown circuits; (E) the inverter load sharing detector circuit; (F) the current-limiting-circuit current transformers; (G) the inverter output filter; (H) the voltage booster and booster filter; (I) the input filter; (J) the voltage regulator magnetic-amplifier; (K) the tuning-fork-oscillator frequency reference; (L) the frequency reference selector circuit; (M) the unijunction-transistor-relaxation-oscillator; (N) the inverter output voltage sensing transformer; (O) the six power rectifiers used for converter operation; and (P) the simple saturable reactor used in the static converter load-division circuit.

The static inverter and converter paralleling methods, and the CUBEX steel quadratic transformer were evaluated during the last half of the third quarter of the contract period. The principles developed during the first three months of the contract were confirmed during these tests. The test results are discussed in detail in the body of this report. Some circuit modifications were

necessary to accomplish the tasks of this contract, but the principles were not changed by the modifications. Those modifications are discussed in detail in the text of this report.

This contract has been extended for five months to include the development of circuits for automatic paralleling and protection of static inverters and converters.

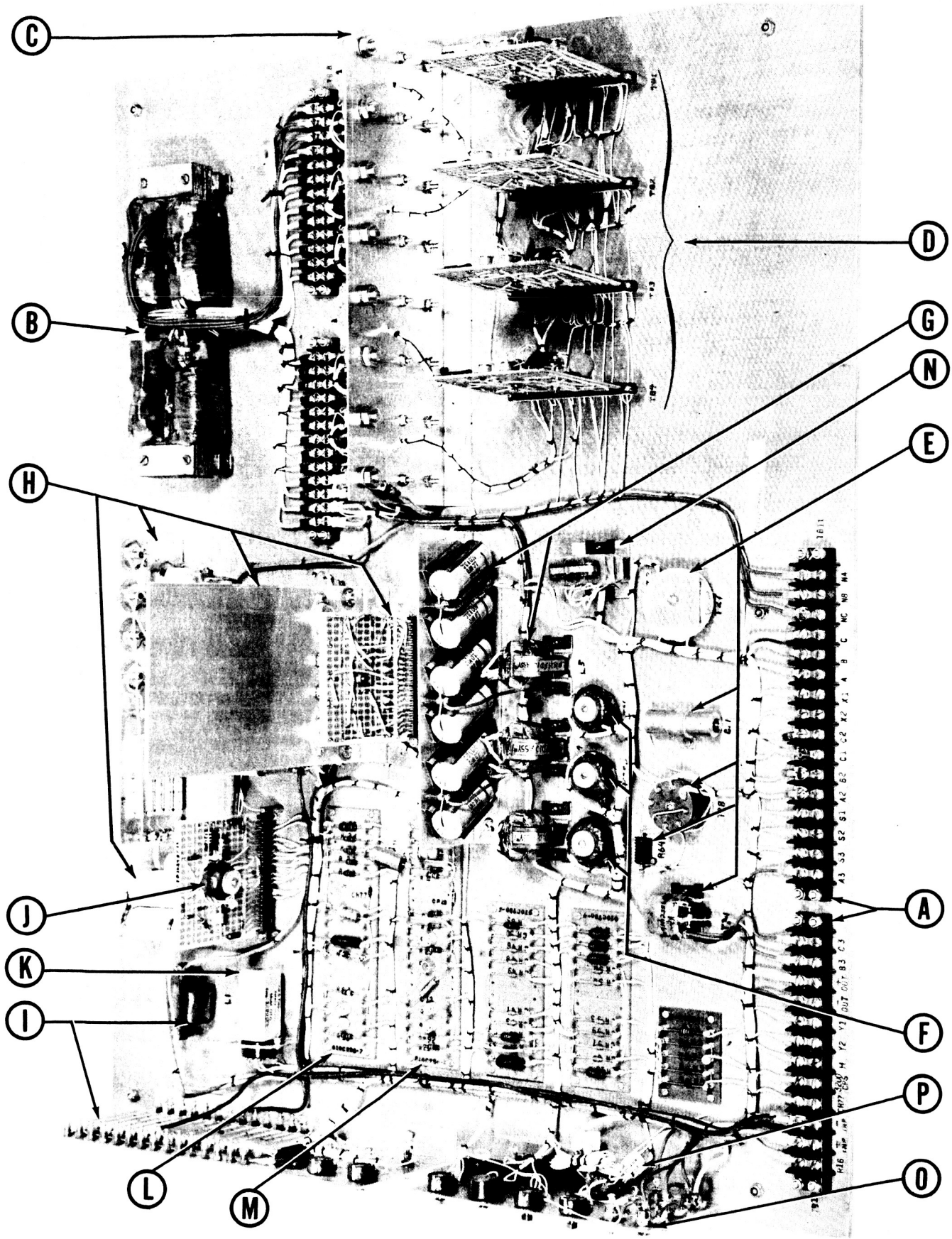


Figure 1. Photograph of One of the Static Inverter/Converter Test Models

II. STATIC INVERTER PARALLELING EVALUATION

The static inverter paralleling evaluation was completed during the third quarter of the contract period. The laboratory set-up is shown in Figure 2. The wiring diagram of the laboratory set-up is shown in Figure 3. Inverter breadboard #2 is shown (A) with its d-c power supply (B), input meters (C), output frequency counter (D), and transformer temperature-rise potentiometer (E). Two complete sets of a-c output voltmeters, ammeters, and wattmeters (F) are located on the center table. The set of a-c output meters in the foreground measured the output of Inverter #2, while the other set measured the output of Inverter #1. The individual load, inverter paralleling, and load paralleling circuit breakers (G) are located on the center table. The load banks (H) and the output frequency counter for inverter #1 (I) are also shown on Figure 2. Inverter #1 is behind the two load banks on a separate table as can be seen in Figure 40.

The results of the paralleling evaluation were very successful. One modification was necessary in the frequency locking circuit and is discussed in the next section. An improved phase locking method became apparent through testing and is discussed in the phase locking section. The test data obtained are discussed in detail in their appropriate sections.

A. Frequency Locking.

The frequency locking circuits were modified before the parallel inverter laboratory tests were begun. Figures 9 and 27 of the first quarterly report show that when two inverters are connected in parallel, the base terminals of both Q23 transistors are connected together. The base of Q23 to the emitter of Q2 (Grd) voltage required to turn on the Darlington connected Q23 and Q2 transistors will most likely be different on each inverter breadboard. The transistor combination which requires the least turn-on voltage will clamp the base drive voltage to the other transistor combination and will be the only one of the two transistor combinations that will operate properly during parallel operation. One of the breadboards would operate at the tuning fork frequency while the other breadboard would operate at its own unijunction-transistor relaxation-oscillator frequency.

The circuit modification consisted of inserting a resistor, designated R72 on Figure 4, between the 3200 cps bus and the base of transistor Q23. The cathode of diode CR92 remains connected to the base of transistor Q23.

The value of R72 was determined experimentally and logically. There are two opposing factors to be considered. One factor is that as the value of resistance increases, the load on the tuning fork oscillator decreases. Hence, as the value of resistance increases the number of inverters that can be synchronized by one tuning fork oscillator also increases. The other factor is that as the value

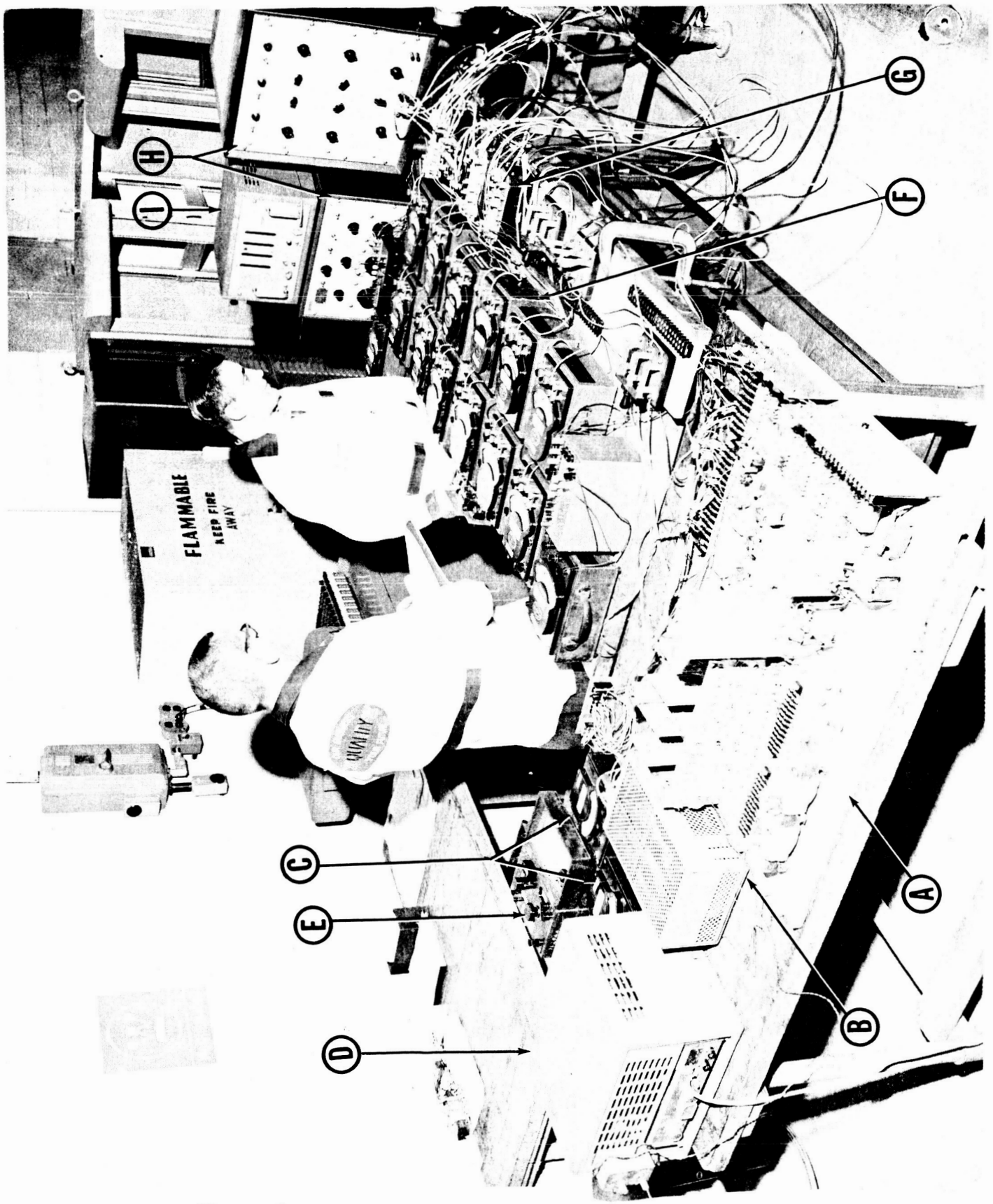


Figure 2. Photograph of Parallel Inverter Laboratory Set-Up

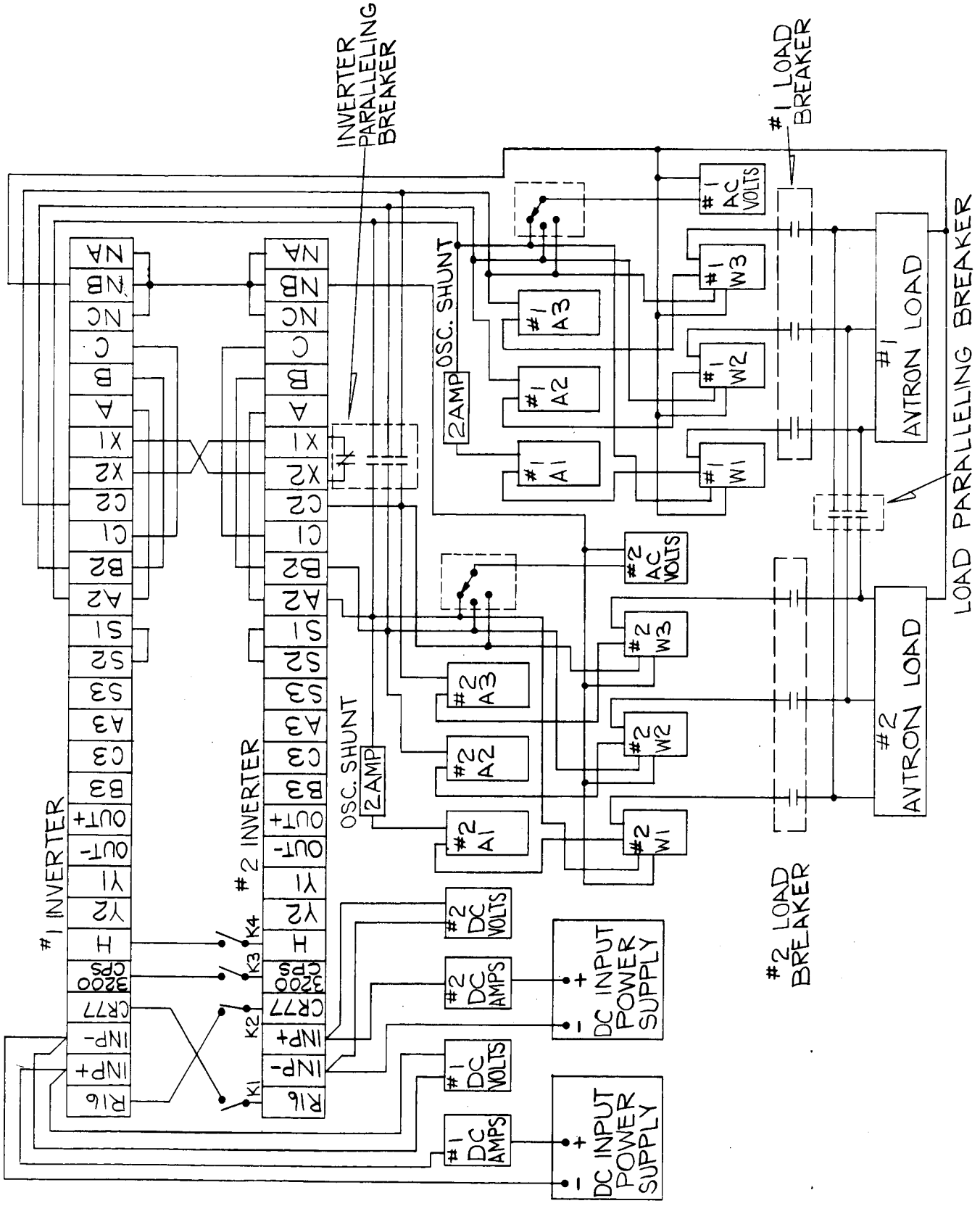


Figure 3. Wiring Diagram of Laboratory Set-Up

of resistance increases, the base drive signal decreases. Therefore, the value of resistance must be low enough to ensure that the base drive signal is always sufficient for proper transistor switching operation. Another consideration is the signal power available from the tuning fork oscillator. The voltage magnitude must be greater than two volts peak-to-peak.

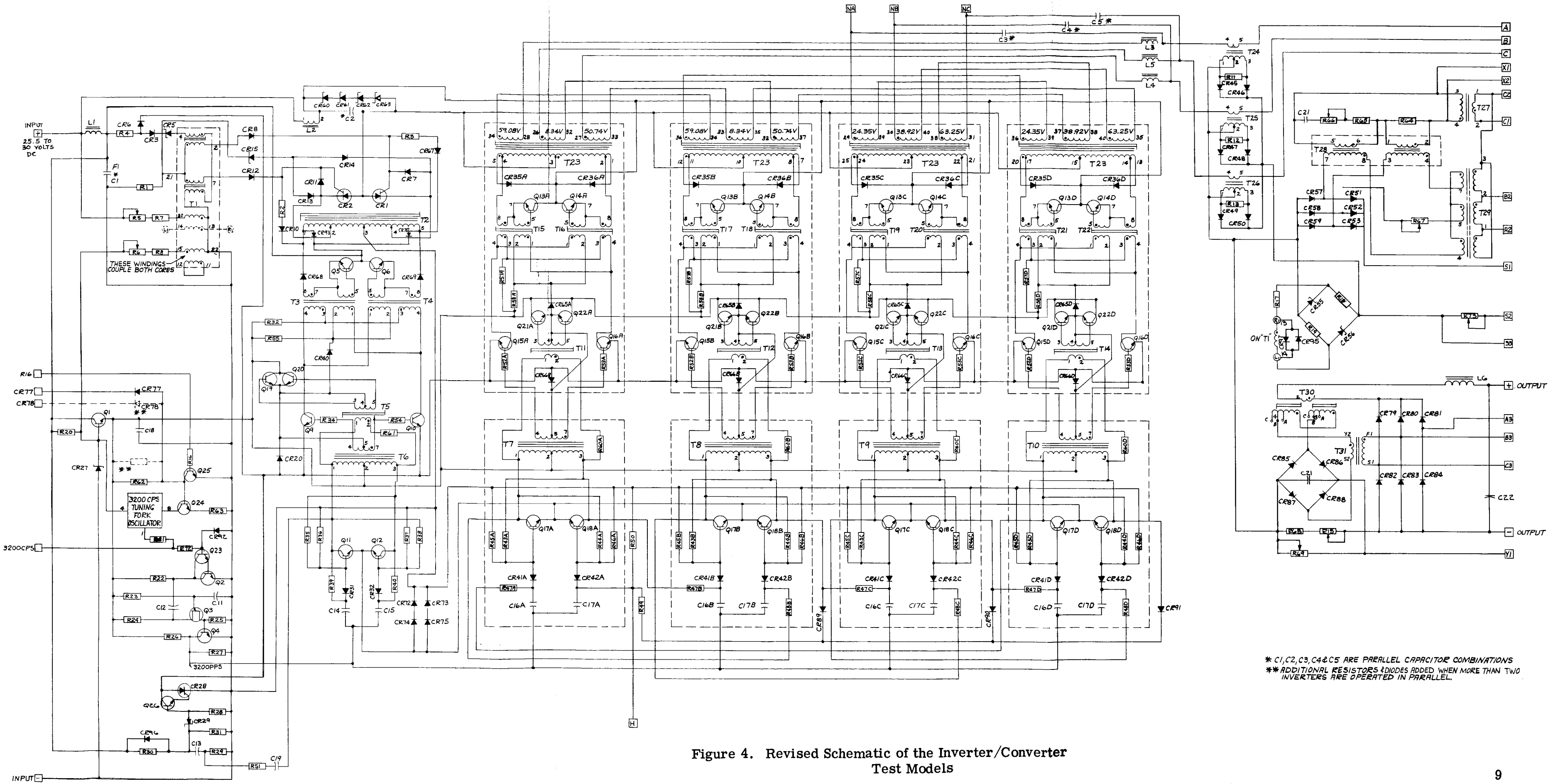
The measured value of resistance that caused the Darlington connected transistors to no longer switch, was 250 K ohms. A standard 47 K ± 10% ohm resistor was selected. Therefore, a factor of safety of about 5 ensures that the tuning fork oscillator signal will always be sufficient to cause the transistor to operate in a switching mode. This value of resistance for R72 will allow about fifty inverters to be synchronized by a single tuning fork oscillator like the ones used on these test models. The tuning fork oscillator used in this study had a peak-to-peak output of 10 volts across a 10 K resistor.

The frequency locking circuits functioned as planned after the modification mentioned above was incorporated. Figure 5 contains the data taken according to paragraph 2 of Appendix I. Appendix I of this report is Appendix II of the second quarterly report, and is included in this report for the reader's convenience. These data verify that one tuning fork is turned on and that the other tuning fork is turned off when two inverters are connected, per that paragraph, with switches K1, K2, and K3 closed.

Figure 6(a) shows the oscilloscope trace of the collector-to-emitter voltage of transistor Q4 on each inverter prior to closing switches K1, K2, and K3. It is obvious that these voltages are not in phase. These voltages are also occurring at slightly different frequencies. The difference frequency between the two tuning fork oscillators was only about 0.04 cps. This small frequency difference is not apparent on this photograph. Figure 6(b) shows these same voltages after switches K1, K2, and K3 are closed. These voltages are in-phase and are occurring at the same frequency.

It should be noted that closing K1, K2, and K3 does not assure that the output voltages of the inverters are in phase. The output voltages are phase locked, but they can be out of phase by $45n°$, where $n = 0, 1, 2, \cdots, 7$. Of course, since n can be zero, the output voltages can be in phase if switches K1, K2, and K3 are closed under certain conditions. The last two statements are strictly true only when both inverters have identical loads. This subject is discussed fully in section IIB.

There are two problems associated with this frequency locking circuit which should be discussed. These problems are related to (1) the long start-up time of tuning fork oscillators and (2) the number of components and interconnections required between paralleled inverters.



* C1, C2, C3, C4 & C5 ARE PARALLEL CAPACITOR COMBINATIONS

** ADDITIONAL RESISTORS & DIODES ADDED WHEN MORE THAN TWO INVERTERS ARE OPERATED IN PARALLEL.

Figure 4. Revised Schematic of the Inverter/Converter Test Models

1565785

K

SUBJECT: INVERTER/CONVERTER MODEL (P/N LYP 18293 T1) SERIAL NO. BB #1 & BB #2

CUSTOMER: ENGRG. DEPT.

S. O. OR TEST NO. N4-202 D. OR L. SPEC. NO. E2N-5I SHAFT NO. LYP 18293 FRAME NO.

TO DETERMINE: FREQUENCY LOCK CIRCUITS Para. 2.0

Para. 2.1 INVERTERS CONNECTED PER FIG. 9.

PARA. 2.7

#1 TUNING FORK OPERATING	#2 TUNING FORK OPERATING
#1 B.B.	#1 B.B.
COLLECTOR Q24 TO GRD = 3.75V	COLLECTOR Q24 TO GRD = 18V
BASE Q24 TO GRD = 4.4V	BASE Q24 " " = 0
BASE Q25 TO GRD = 0	BASE Q25 " " = .75V
#2 B.B.	#2 B.B.
COLLECTOR Q24 TO GRD = 18.5V	COLLECTOR Q24 TO GRD = 3.7V
BASE Q24 " " = 0	BASE Q24 " " = 4.4V
BASE Q25 " " = .75V	BASE Q25 " " = 0

PARA. 2.8 OK SEE ABOVE PARA 2.7

PARA 2.9 OK PICTURE #1 SHOWS INVERTERS OPERATING AT ITS OWN TUNING FORK FREQUENCY. COLLECTOR OF Q4 TO GRD. PICTURE #2 SHOWS BOTH INVERTERS OPERATING AT TUNING FORK #2 FREQUENCY

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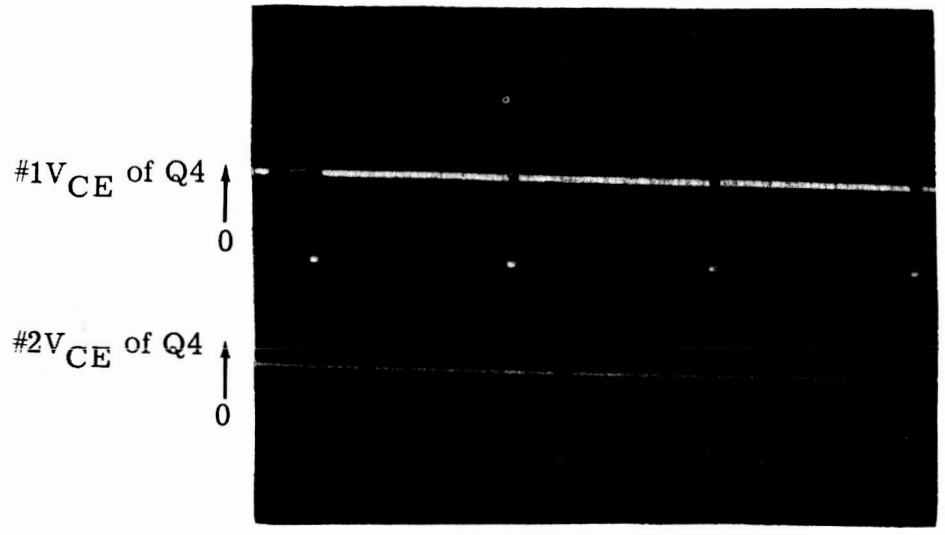
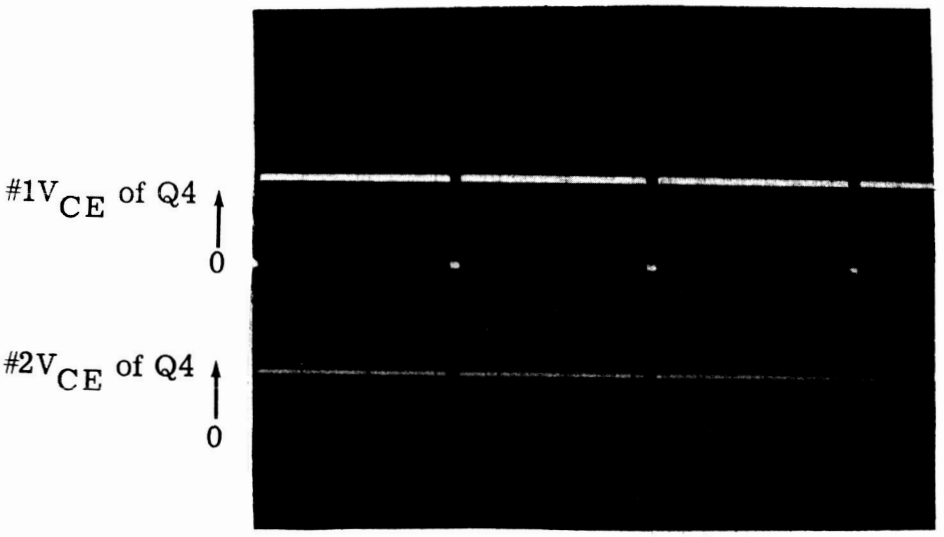
Figure 5. Characteristics of the Frequency Locking Circuits



(a)



(b)

Figure 6. Photographs of the Oscilloscope Tracing of the Collector-to-Emitter Voltage of Transistor Q4 on Each Inverter (a) Prior to Closing Switches K1, K2, and K3 and (b) After Closing Switches K1, K2, and K3.

The long start-up time (two to four seconds) of a tuning fork oscillator presents a problem if the tuning fork oscillator that is operating in a paralleled system should fail. The failed tuning fork oscillator must be shut off and one of the other tuning fork oscillators must be started. The inverters must be unparalleled during the transition period since each inverter would be operating at its own unijunction-transistor relaxation-oscillator frequency. The use of faster starting oscillators such as crystal oscillators, multivibrators, etc., would shorten the transition period considerably. It should be noted that a parallel inverter system will always be disturbed for at least a fraction of a second if the operating frequency reference should fail. It would be impossible to switch to another frequency reference instantly and to have the new frequency reference operate at the same frequency and in phase with the voltage pulses that would have occurred if the first frequency reference had not failed. Design effort should be used to minimize the duration of this disturbance.

The second problem associated with the frequency locking method is that, for each additional inverter that is inserted in a parallel inverter system, a resistor and a diode must be added to every inverter in the parallel system. For a parallel inverter system having n inverters, there must be n-1 such resistors and n-1 such diodes in each of the inverter frequency locking circuits.

The main reason for concern is that, with this frequency locking method, the number of interconnections between inverters increases as the number of inverters in the system increases. Hence, as the number of necessary interconnections increases, the reliability of these interconnections decreases.

Another important consideration is that the maximum number of static inverters of a given design which can be operated in parallel is limited by the number of resistors and diodes in each frequency locking circuit. It would be more desirable to be able to parallel an unlimited number of static inverters of a given design. In this way, a standard inverter design could be utilized in a wide variety of applications.

A practical solution to this problem is available and is recommended for all future work in this area. The practical solution to this problem is to use a single frequency reference which is physically separated from all of the inverters. The frequency reference should contain as many frequency standards as required to meet the desired reliability with a "frequency locking circuit" similar to the one used in this study. A new "frequency locking circuit" could be developed which allows all of the frequency standards to operate continuously. The circuit used in this study shuts off all but one of the frequency standards. Such a new circuit would by-pass the disadvantage of the long start-up time of a tuning fork oscillator mentioned above and would minimize the frequency disturbance which results from changing frequency standards.

Each inverter package should contain its own unijunction-transistor relaxation-oscillator or some other type oscillator, which can be synchronized with the frequency reference. Then each inverter can be operated unparalleled and independent of the frequency reference if the frequency reference were to fail completely. A unijunction-transistor relaxation-oscillator can be accurate to about ±1%. The number of necessary interconnections between the inverters would not be affected by the number of inverters in the parallel system. The number of components in each inverter would not be affected by the number of inverters in the parallel system. Therefore, a standard inverter of this type could be built and operated independently or in parallel with an unlimited number of similar inverters.

B. Phase Locking.

The phase locking circuits functioned properly. Figure 7 identifies the oscilloscope traces shown in Figure 8.

The method of closing switch K4 to lock the inverter countdown circuits in-phase is undesirable from a system transient standpoint. As mentioned previously, when the frequency locking circuits are energized, the output voltages can be out of phase by 45n°, n = 0, 1, 2, ···, 7. When switch K4 is closed, one or both of the countdown circuits in the inverters must be disturbed and, as described in the first quarterly report (pp. 23-26), must shift until both countdown circuits operate in-phase with each other. The output voltages will be disturbed during this period of time. If switches K1, K2, and K3 are closed at random, there is no way of knowing which one (or if both) of the countdown circuits will change when switch K4 is closed. Thus, the system load voltage could be distorted for as long as one output cycle while the two inverters are getting in-phase with each other. This is not harmful to the inverters but could be detrimental to the proper operation of gyro-motors or other frequency sensitive devices operating on the bus.

This phase locking transient can be completely eliminated if switches K1, K2, and K3 are initially closed only at an instant when the two inverter countdown circuits are in-phase with each other. By locking the inverter frequencies together at that instant, the inverters will remain in phase with each other without closing switch K4. Because of the very small frequency difference between the two inverter frequency references, this method of simultaneous frequency and phase locking was experimentally verified in the laboratory by manually closing switches K1, K2, and K3 when the two inverter countdown circuits were observed (on a dual channel oscilloscope) to be in phase with each other. For output frequency differences above about 0.1 cycle per second, it would be impossible to physically observe the proper paralleling conditions and manually close switches K1, K2, and K3 at the proper instant. One of the reasons for extending this contract is to develop an electrical circuit which will automatically sense the correct instant for paralleling and will perform the functions

K1565786

SUBJECT INVERTER/CONVERTER MODEL (P/N LVP18293T1)

CUSTOMER ENGRG. DEPT. SERIAL NO. BB#1

S. O. OR TEST NO. N4-202 S. ORD. NO. E2N-5I DRAFT NO. LVP18293 FRAME NO. BB#2

TO DETERMINE PHASE LOCK CIRCUITS PARA 3.0

CONNECTED PER FIG. 9.0

PARA. 3.1 PICTURE #3 SHOWS COLLECTOR OF Q19A TO GRD VOLTAGE ON BOTH INVERTERS OPERATING AT THE SAME FREQUENCY BUT NOT IN PHASE.

PARA. 3.2 PICTURE #4 SHOWS COLLECTOR OF Q19A TO GRD. VOLTAGE ON BOTH INVERTERS OPERATING AT THE SAME FREQUENCY AND IN PHASE.

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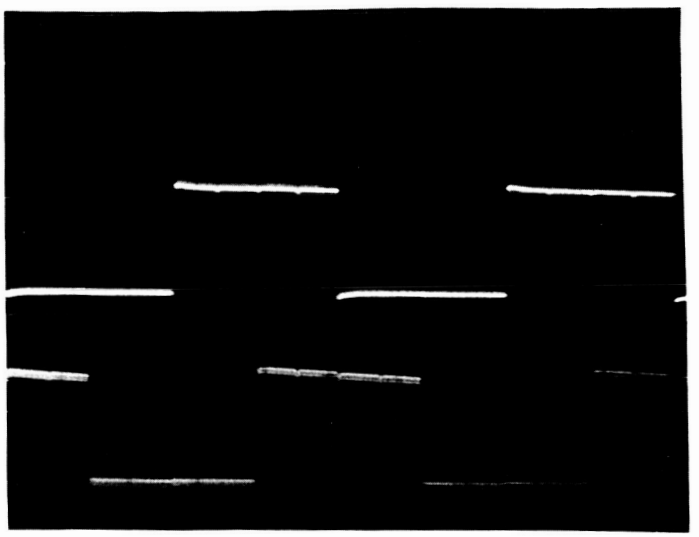
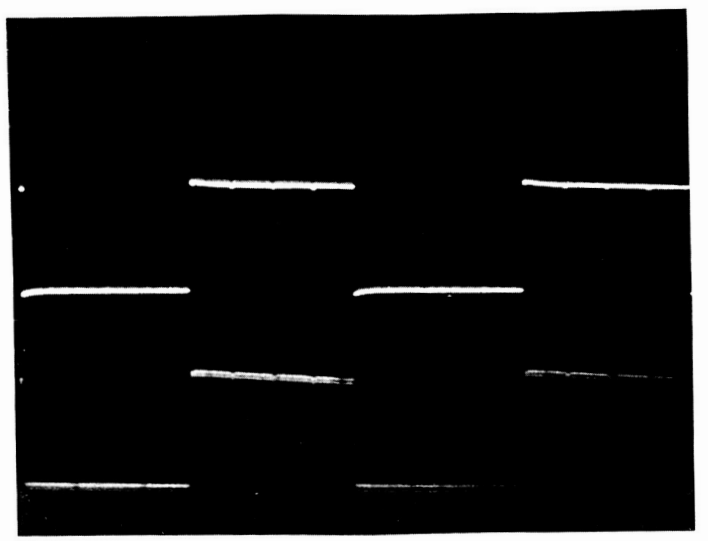
Figure 7. Description of Photographs on Figure 8 Which Illustrate the Effect of the Phase Locking Circuits



time ⟶ (Picture #3)

(a) Switches K1, K2, and K3 closed.



time ⟶ (Picture #4)

(b) Switches K1, K2, K3, and K4 closed.

Figure 8. Photographs of the Oscilloscope Tracing of the Collector-to-(-inp) Voltage of Transistor Q17A on Each Inverter Showing (a) the Inverters Operating at the Same Frequency but Out of Phase and, (b) the Inverters Operating at the Same Frequency and In Phase

equivalent to closing switches K1, K2, and K3. This automatic paralleling circuit must then determine if the two countdown circuits remained in phase with each other and then close the circuit breaker which connects the inverter output terminals in parallel.

Conventional methods for the automatic paralleling of rotating a-c generators all rely on observations of the corresponding generator terminal voltages to determine if two generators are near enough in phase to be paralleled. This method is not sufficiently accurate for paralleling static inverters because of the static inverter internal impedance. For example, if two identical isolated static inverters are dissimilarly loaded and their respective output voltages are exactly in phase with each other, the two countdown circuits will not be in phase with each other. For this reason, the static inverter terminal voltages cannot be used to determine if two countdown circuits are in phase with each other. Fortunately this can be very easily determined with simple static logic circuits. Two inverter countdown circuits are in phase with each other and can be connected to the same frequency reference during the periods when transistors Q4, Q18A, Q18B, Q18C, and Q18D of both inverters are conducting. This can be determined by a simple "NOR" circuit. This automatic paralleling circuit will be developed and demonstrated experimentally during the extension of this contract.

C. Load Division.

The data taken during the parallel inverter tests show that the load division circuit performance met or exceeded the performance specified in the first quarterly report. These data will be discussed in detail in the following paragraphs.

1. Load Division Circuit Gain.

The load division circuit gain data are shown in Figure 9 (Breadboard #1) and Figure 10 (Breadboard #2). These data were taken according to Appendix I, Paragraph 1.0. The value of the load division circuit gain was to have been:

$$\frac{\partial E}{\partial I_{DQ}} = -0.412 \text{ Volts/Ampere} \quad \text{(first quarterly report, Pages 27 \& 28).}$$

The value obtained from the data is:

$$\frac{\partial E}{\partial I_{DQ}} = -\left(1 - \frac{63.4}{115.1}\right) = -0.45 \text{ Volts/Ampere;}$$

where $63.4 = \frac{63.8 + 64.7 + 61.7}{3}$,

K 1565778

SUBJECT Inverter/Converter Model (P/N LYP 18293 J1)

CUSTOMER Engrg. Dept. SERIAL NO. BB #1

S. O. OR TEST NO. NH-202 D. OR E. SPEC. NO. E2N-5J SHAFT NO. LYP 18293 FRAME NO.

TO DETERMINE Feasibility Of Paralleling Inverters & Converters

Para 1.0 Measurement Of Reactive Load Division Circuit Loop Gain

	Output	
V1-N	115.8	63.8
V2-N	114.5	64.7
V3-N	115.0	61.7
A1	0	2.18
A2	0	2.18
A3	0	2.11
W1	0	69
W2	0	70
W3	0	65
P.F.	–	.5 Lag.
	Input	
DC Amps	3.4	16.9
DC Volts	29.4	28.7

PREVIOUS TEST PAGE — DATE Feb 25, 1964 — SIGNED W. Miller & R. Ridenour — ENGINEER IN CHARGE G.W. Ebersberger

Figure 9. Data Taken to Measure the Reactive Load Division Circuit Loop Gain of Inverter Breadboard #1

K 1565780

SUBJECT INVERTER/CONVERTER MODEL (P/N LYP18293-1)

CUSTOMER ENGRG. DEPT. SERIAL NO. B.B.#2

S. O. OR TEST NO. N4-202 D. OR L. SPEC. NO. E2N-5J SHAFT NO. LYP18293 FRAME NO.

TO DETERMINE

PARA 1.0 MEASUREMENT OF REACTIVE LOAD DIVISION LOOP GAIN

V1-N		116		91.	79	67	63.8							
V2-N		115.2		90.8	78.5	67	63							
V3-N		114.4		90.8	79	67	62.8							
A1		0	.5	1.0	1.5	2.02	2.2							
A2		0	.5	1.0	1.48	1.99	2.17							
A3		0	.5	1.0	1.5	2.0	2.15							
W1		0		40	55	65	67							
W2		0		40	55	65	66							
W3		0		40	55	63	64							
PF		—		.5	.5	.5	.5 LAG							
DC AMPS		3.4		8.	10.5	12.8	13.4							
DC VOLTS		29.75		29.5	28.8	28.75	28.75							

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Figure 10. Data Taken to Measure the Reactive Load Division Circuit Loop Gain of Inverter Breadboard #2

and $115.1 = \frac{115.8+114.5+115.0}{3}$.

These data are taken from Figure 9. The data from Figure 10 give:

$$\frac{\partial E}{\partial I_{DQ}} = -(1 - \frac{63.2}{115.2}) = -0.451 \text{ Volts/Ampere.}$$

So, the load division circuit gain exceeds the value specified in the first quarterly report.

2. Load Division with Balanced Three-Phase Loads.

Figures 11 through 14 contain data taken with the inverters operating in parallel with balanced loads of various magnitudes and power factors. Both inverters terminal voltages were initially adjusted to 115 volts rms (L-N). The data show that the inverters load difference was lowest with a 0.75 lagging PF load and highest with a 0.9 leading power factor load. Even the worst case is well within the 10% unbalance from the average which was specified as an objective on Page 77 of the first quarterly report.

Figure 15 gives the calibration and recording oscillograph data for Figures 16 through 21. Figure 16 and Figure 17 are calibration tracings. Figures 18 through 21 show the transients encountered when the inverters are paralleled with 100% loads of four different power factors on each inverter. The transients are almost non-existent. The small d-c signal at the bottom of the trace indicates whether the inverters are paralleled or not. A positive d-c voltage indicates that the paralleling breaker is closed. It should be noted that the X1 - X2 terminals (Figure 4) should be shorted together whenever isolated (or single) inverter operation is desired. Figure 22 contains the data for Paragraphs 4.12 and 4.13 of Appendix I. The data in the first two columns and their associated oscillograph, Figure 23, show that an unloaded inverter can be paralleled with a loaded inverter. The transient lasts about 30 milliseconds. The data in the last two columns of Figure 22 and their associated oscillograph Figure 24, show that the inverters can be paralleled at no load, then have the equivalent of twice rated load for one inverter suddenly applied and removed with no undesirable effects. Note that the inverters share load during the load on transient. The rated load application and removal transients last about 50 milliseconds.

K 1565793

SUBJECT INVERTER/CONVERTER (P/N LYP18293 J1) SERIAL NO. BB #1

CUSTOMER ENGR. DEPT. FRAME NO. BB #2

S. O. OR TEST NO. N4-202 ~~S. OR L. SPEC NO.~~ E2N-5J SHAFT NO. LYP18293

TO DETERMINE PARALLEL INVERTER OPERATION PARA. 4.0

Para 4.10.

#1 V1-N	115.5	115.8	115.8	115.	115.2	114.5		WESTON MODEL 341				
#1 V2-N	115.1	115.2	115.5	115.5	115.	114.			# 17957			
#1 V3-N	114.5	115	115.5	115.8	115.2	114.5			C-R 150			
#1 A1	0	.55	1.09	1.65	2.15	2.75		WESTON M370	# 9985	C-R 5		
#1 A2	0	.5	1.09	1.64	2.18	2.8		"	"	# 9991	"	
#1 A3	0	.5	1.05	1.55	2.08	2.64		"	"	# 10293	"	
#1 W1	1	58	123	190	248	315		"	M310	# 14344	C-R 5	
#1 W2	6	56	123	192	251	320		"	"	# 14756	"	
#1 W3	5	55	125	177	238	300		"	"	# 14754	"	
#1 DC AMPS	3.3	10.3	18.0	28.0	37.5	49.9		(W)	TYPE PXS	# 2600416	C-R 50	
#1 DC VOLTS	29.8	29.3	28.9	28.3	27.7	26.9		(W)	"	# 1517824	C-R 30	
#1 FREQ.	400	400	400	400	400	400		BERKLEY EPUT METER	M5556P	# 314		
#2 V1-N	115.5	115.8	115.8	115.0	115.2	114.5		WESTON MODEL 341				
#2 V2-N	115.	115.	115.5	115.5	115.	114			# 14999			
#2 V3-N	114.5	115	115.5	115.5	115.2	114.5			C-R 150			
#2 A1	0	.6	1.08	1.66	2.15	2.72		WESTON M370	# 5589	C-R 5		
#2 A2	0	.6	1.1	1.62	2.12	2.65		"	"	# 9989	"	
#2 A3	0	.6	1.1	1.71	2.23	2.83		"	"	# 9914	"	
#2 W1	4	65	125	195	252	315		"	M310	# 13854	C-R 5	
#2 W2	9	65	126	188	244	304		"	"	# 13856	"	
#2 W3	5	65	131	196	257	325		"	"	# 15923	"	
#2 DC AMPS	4.5	11.8	20.	29.4	39.5	49.		(W)	TYPE PXS	# 1975462	C-R 50	
#2 DC VOLTS	29.8	29.3	28.8	28.1	27.6	26.9		(W)	"	# 2600591	C-R 30	
#2 FREQ	400	400	400	400	400	400		BERKLEY EPUT METER	M5556P	# 317		
PF	—	1.0	1.0	1.0	1.0	1.0						
% LOAD	0	25	50	75	100	125						

SEE PAGE K1565787 FOR TEST CIRCUIT SCHEMATIC

PREVIOUS TEST PAGE 3-5-64 DATE Marlon-Stevenson SIGNED G. ERNSBERGER ENGINEER IN CHARGE

Figure 11. Characteristics of Parallel Inverter Operation with 1.0 P.F. Loads

K 1565791

SUBJECT INVERTER/CONVERTER (P/N LYP 18293 J1)

CUSTOMER ENGG. DEPT. SERIAL NO. B.B. #1

S. O. OR TEST NO. N4-202 S. OR SPEC. NO. E1N-5J- SHAFT NO. LYP/18293 FRAME NO. B.B. #2

TO DETERMINE PARALLEL INVERTER OPERATION PARA 4.0

		PARA 4.10											
#1 V1-N		115.1	115.	115.2	116	116.5	112.5						
#1 V2-N		115.2	115.5	115.2	115	115.	111.						
#1 V3-N		115.	115.1	115.5	116	116	112.5						
#1 A-1		0	.6	1.09	1.65	2.18	2.76						
#1 A-2		0	.55	1.05	1.65	2.19	2.75						
#1 A-3		0	.6	1.05	1.63	2.18	2.66						
#1 W-1		0	46	93	140	183	231						
#1 W-2		0	45	96	145	191	236						
#1 W-3		0	40	93	139	186	236						
#1 DC AMPS		3.	8.7	15.3	22.1	29.5	37.						
#1 DC VOLTS		29.9	29.5	29.1	28.7	28.3	27.8						
#1 FREQ.		400	400	400	400	400	400						
#2 V1-N		115	115	115.2	116	116.5	112.5						
#2 V2-N		115.2	115.5	115.2	115	115	111.						
#2 V3-N		115.1	115.1	115.5	116	116	112.5						
#2 A-1		0	.65	1.1	1.63	2.15	2.67						
#2 A-2		0	.65	1.09	1.62	2.11	2.66						
#2 A-3		0	.7	1.1	1.66	2.19	2.75						
#2 W-1		0	49	100	145	192	236						
#2 W-2		0	47	94	135	175	218						
#2 W-3		0	49	97	145	188	236						
#2 DC AMPS		4.4	9.8	16.2	23.5	29.9	37.						
#2 DC VOLTS		29.8	29.4	29.	28.6	28.1	27.8						
#2 FREQ		400	400	400	400	400	400						
P.F.		.~~6~~	.75	.75	.75	.75	.75						
LOAD		0	25	50	75	100	125						

SEE PAGE K 1565793 FOR METER DATA

SEE PAGE K 1565787 FOR TEST CIRCUIT SCHEMATIC

PREVIOUS TEST PAGE

3-5-64 DATE

Marbes-Stevenson SIGNED

G. ERNSBERGER ENGINEER IN CHARGE

Figure 12. Characteristics of Parallel Inverter Operation with 0.75 Lagging P.F. Loads

K1565795

SUBJECT INVERTER \ CONVERTER (P/N LYP18293 J1)

CUSTOMER ENGRG. DEPT. SERIAL NO. B.B. #1

S. O. OR TEST NO. N4-202 DWG. OR SPEC. NO. E1N-5J- SHAFT NO. LYP18293 FRAME NO. B.B. #2

TO DETERMINE PARALLEL INVERTER OPERATION PARA 4.0

			PARA	4.10.									
#1	V1-N		116	115.1	115.7	115.9	116.2	112.9					
#1	V2-N		115.1	115.2	115.5	115.1	115.	111.8					
#1	V3-N		114.8	115.	115.5	116.	116.2	113.					
#1	A-1		0	.55	1.08	1.66	2.2	2.75					
#1	A-2		0	.51	1.05	1.66	2.2	2.76					
#1	A-3		0	.55	1.05	1.64	2.15	2.65					
#1	W-1		0	53	110	168	225	282					
#1	W-2		0	55	111	173	230	285					
#1	W-3		0	54	106	165	220	272					
#1	DC AMPS		3.0	9.8	16.9	25.5	34.8	39.3					
#1	DC VOLTS		29.9	29.5	29.1	28.6	27.9	27.4					
#1	FREQ.		400	400	400	400	400	400					
#2	V1-N		116	115.1	115.7	115.9	116.2	112.9					
#2	V2-N		115	115.2	115.5	115.1	115	111.8					
#2	V3-N		114.8	115	115.5	116	116.2	113.					
#2	A-1		0	.56	1.06	1.66	2.16	2.68					
#2	A-2		0	.56	1.06	1.64	2.12	2.64					
#2	A-3		0	.6	1.1	1.7	2.22	2.78					
#2	W-1		0	60	115	174	229	283					
#2	W-2		0	58	111	165	215	266					
#2	W-3		0	57	115	165	230	287					
#2	DC AMPS		4.5	11.0	18.5	27.5	35.2	44.1					
#2	DC VOLTS		29.8	29.3	28.8	28.3	27.8	27.4					
#2	FREQ		400	400	400	400	400	400					
	P.F.		—	.9	.9	.9	.9	.9	LAG.				
	%LOAD		0	25	50	75	100	125					

SEE PAGE K1565793 FOR METER DATA

SEE PAGE K1565787 FOR TEST CIRCUIT SCHEMATIC

PREVIOUS TEST PAGE

3-5-64 DATE

Marker-Stevenson SIGNED

G. ERNSBERGER ENGINEER IN CHARGE

Figure 13. Characteristics of Parallel Inverter Operation with 0.9 Lagging P.F. Loads

K

SUBJECT INVERTER \ CONVERTER (P/N LYP18213-)

CUSTOMER ENGRG. DEPT. SERIAL NO. B.B. #1

S. O. OR TEST NO. N4-202 SPEC. NO. E2N-5J. SHAFT NO. LYP 18299 FRAME NO. B.B. #1

TO DETERMINE PARALLEL INVERTER OPERATION PARA 4.0

			PARA		4.10.									
#1	V1-N		116.1	116	115.9	115.8	114.5	113.5						
#1	V2-N		115.	114.5	115.	114.7	114.9	112.5						
#1	V3-N		115.	115.2	114.8	114.8	115.5	113.						
#1	A-1		0	.55	1.05	1.6	2.1	2.67						
#1	A-2		0	.5	1.05	1.65	2.16	2.74						
#1	A-3		0	.5	1.02	1.55	2.0	2.58						
#1	W-1		0	52	109	167	220	276						
#1	W-2		0	45	104	164	226	271						
#1	W-3		0	49	100	158	206	263						
#1	D.C. AMPS		3.3	9.0	17.5	26.1	34.	44.1						
#1	D.C. VOLTS		29.1	29.7	29.1	28.5	28.1	27.4						
#1	FREQ.		400	400	400	400	400	400						
#2	V1-N		116.1	116	115.9	115.8	114.5	113.5						
#2	V2-N		115	114.5	115.	114.7	114.9	112.5						
#2	V3-N		115	115.2	114.8	114.8	115.5	113.						
#2	A-1		0	.55	1.1	1.65	2.25	2.77						
#2	A-2		0	.55	1.1	1.66	2.22	2.73						
#2	A-3		0	.6	1.2	1.8	2.35	2.9						
#2	W-1		0	61	117	176	242	288						
#2	W-2		0	65	121	182	242	287						
#2	W-3		0	62	119	188	248	296						
#2	D.C. AMPS		4.5	11.5	19.	28.2	38.1	48.						
#2	D.C. VOLTS		29.6	29.2	28.7	28.2	27.7	27.1						
#2	FREQ.		400	400	400	400	400	400						
	P.F.		-	.9	.9	.9	.9	.9	LEADING.					
	% LOAD		0	25	50	75	100	125						

SEE PAGE K 1565793 FOR METER DATA

SEE PAGE K 1565787 FOR TEST CIRCUIT SCHEMATIC

PREVIOUS TEST PAGE 3-5-64 DATE Marlin Thorson SIGNED G. ERNSBERGER ENGINEER IN CHARGE

Figure 14. Characteristics of Parallel Inverter Output with 0.9 Leading P.F. Loads

K1565797

SUBJECT: INVERTER \ CONVERTER (P/N LYP18293JD)

CUSTOMER: ENGR DEPT — SERIAL NO.: B.B. # 1

S. O. OR TEST NO.: M4-102 — D. SPEC. NO.: E2N-5J- — DRAWING NO.: LYP18293 — FRAME NO.: B.B. #2

TO DETERMINE: PARALLEL INVERTER OPERATION PARA 4.0

PARA. 4.11.

CAL. #4 #1 VI-N 115V / 1.15 IN — #1 AI 20A / 1 in. — #2 VI-N 115V / 1.15 IN — #2 AI 20A / 1 IN.

#2 PARALLEL AT 100% 1.0 PF ON EACH UNIT

3 PARALLEL AT 100% .75 PF ON EACH UNIT.

4 PARALLEL AT 100% .9 PF LAGGING ON EACH UNIT

5 PARALLEL AT 100% .9 PF LEADING ON EACH UNIT

SEE PAGE K1565787 FOR TEST CIRCUIT SCHEMATIC

SEE PAGE K1565793 FOR METER DATA

CAMERA SPEED 33 IN. PER SEC.

CENTURY OSCILLOGRAPH MODEL 408 Ser. # 284

TRACE	Elem. No.	ELE. PO.	FREQ.	Coil RES.	DEFL. MA/IN	ATT. RES.
#1 VI-N	W334	1	2000	46.2Ω	41.9	2511Ω
# 1 AI	W213	5	510	43.4Ω	3.13	161Ω
#2 VI-N	A0102	7	2000	45.9Ω	47.3	5111Ω
#2 AI	W646	21	510	45.9Ω	3.33	171Ω
PARALLEL SER. SIGNAL	Y540	17	1200	45.7Ω	18.5Ω	11111Ω

PREVIOUS TEST PAGE — DATE: 3-7-64 — SIGNED: R. Marden C. Stevenson — ENGINEER IN CHARGE: G. ERNSBERGER

Figure 15. Description of the Oscilloscope Recordings of Figures 16 through 21, and Data for Oscillograph Calibration

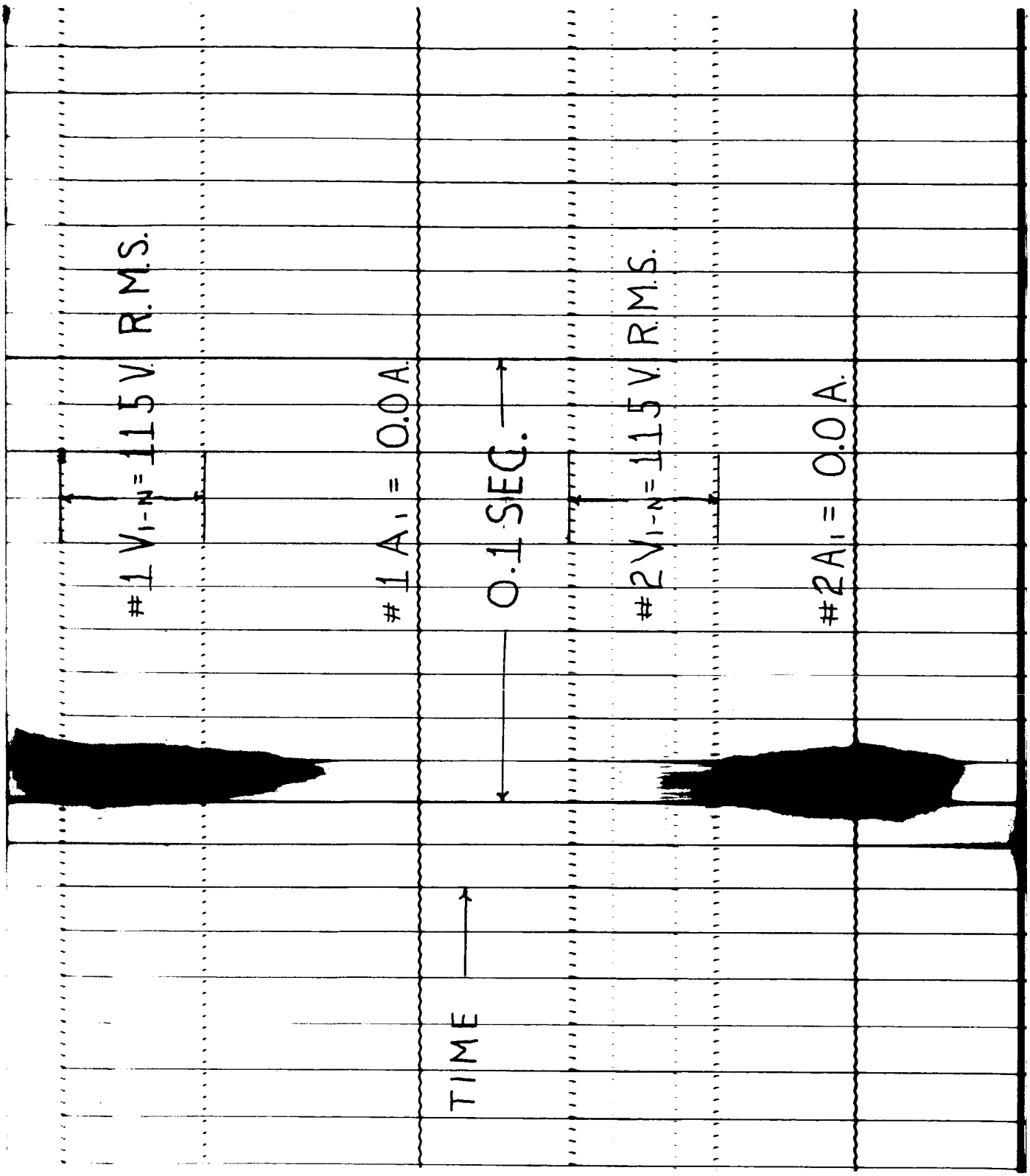

Figure 16. Inverter Voltage Calibration Oscillograph Recording (Osc. #1)

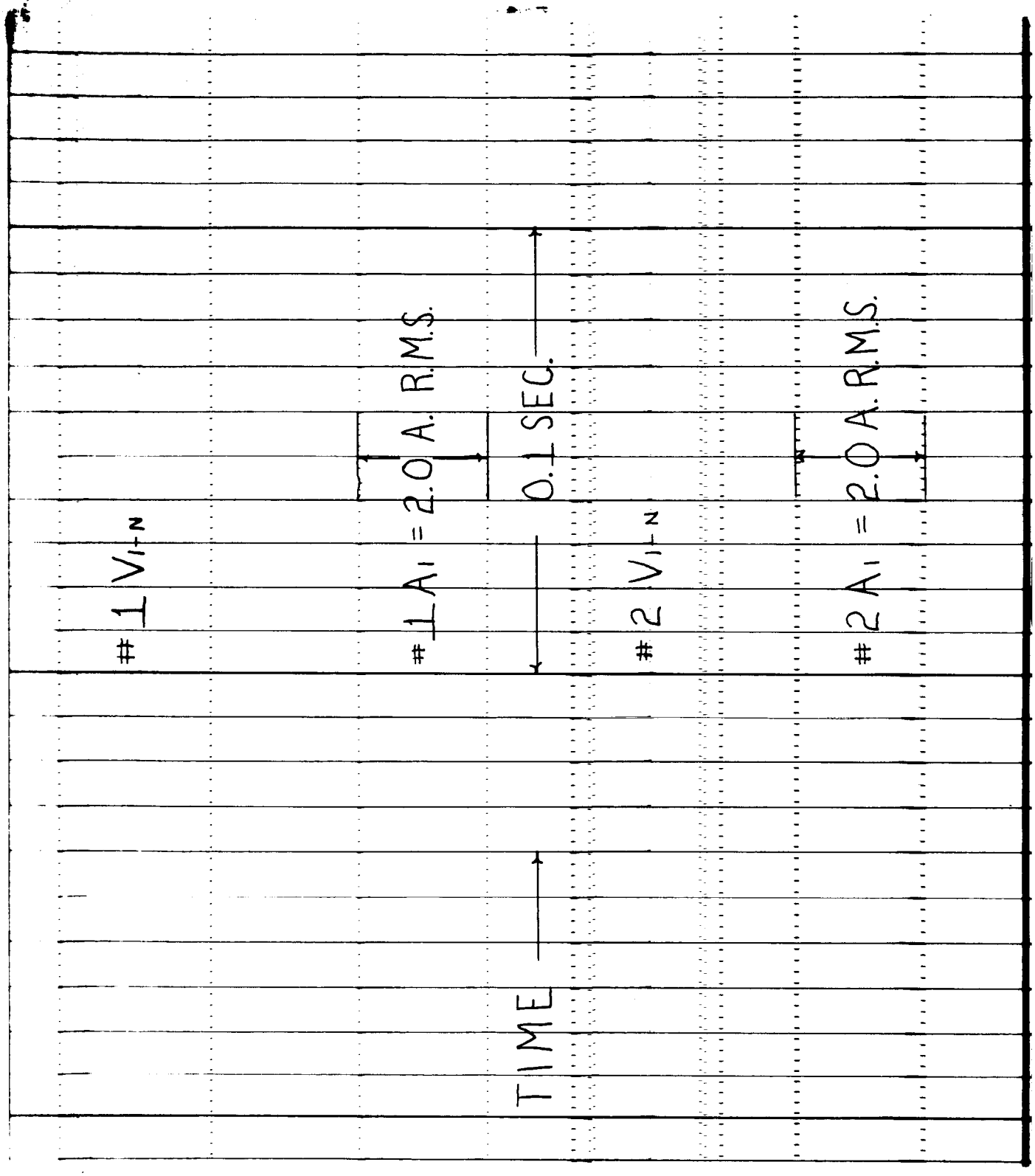

Figure 17. Inverter Current Calibration Oscillograph Recording (Osc. #1)

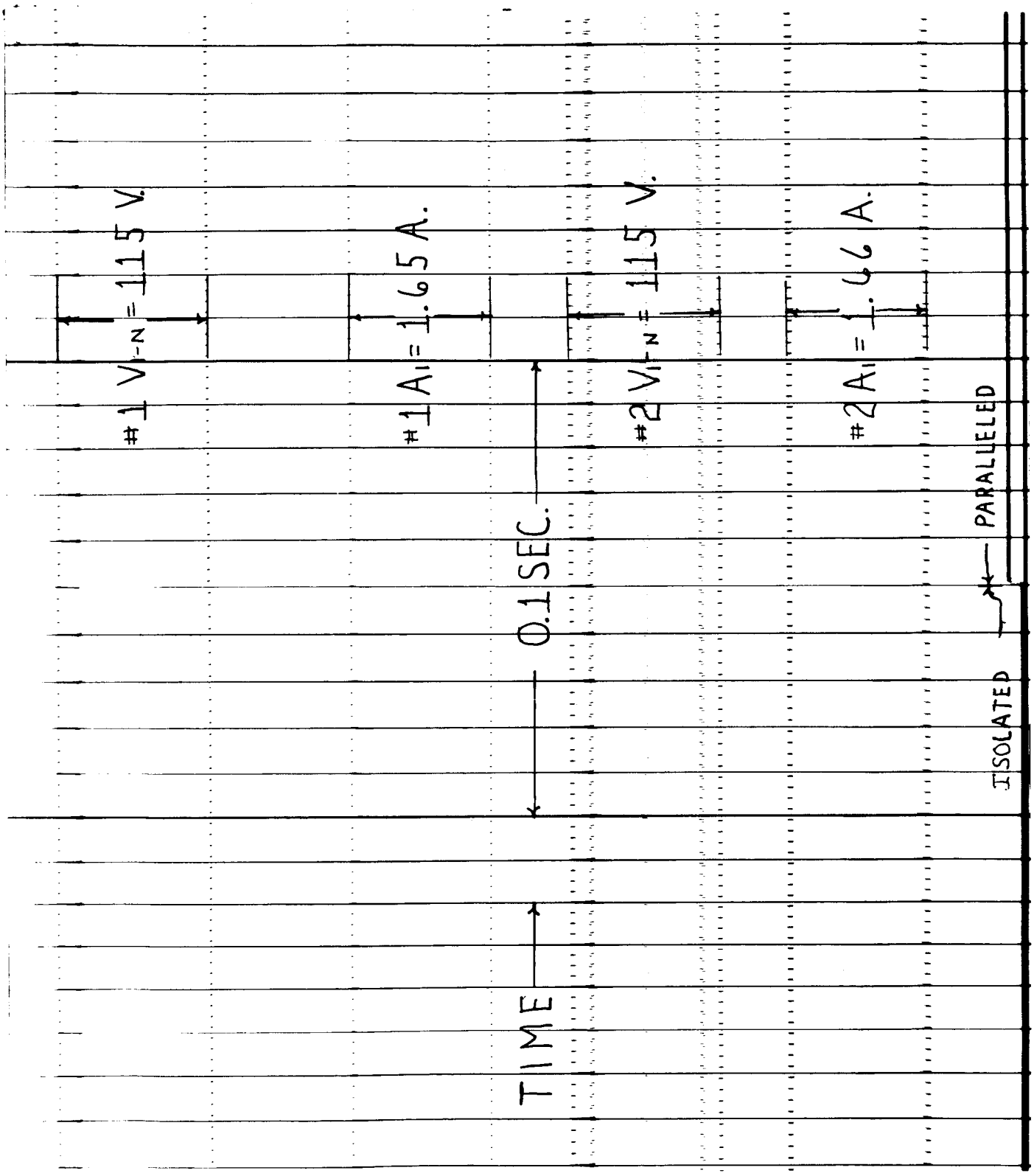

Figure 18. Oscillograph Recording of the Transient Caused by Paralleling Two Inverters. Each Inverter had a 100%, 1.0 P. F. Load on it Prior to Paralleling (Osc. #2)

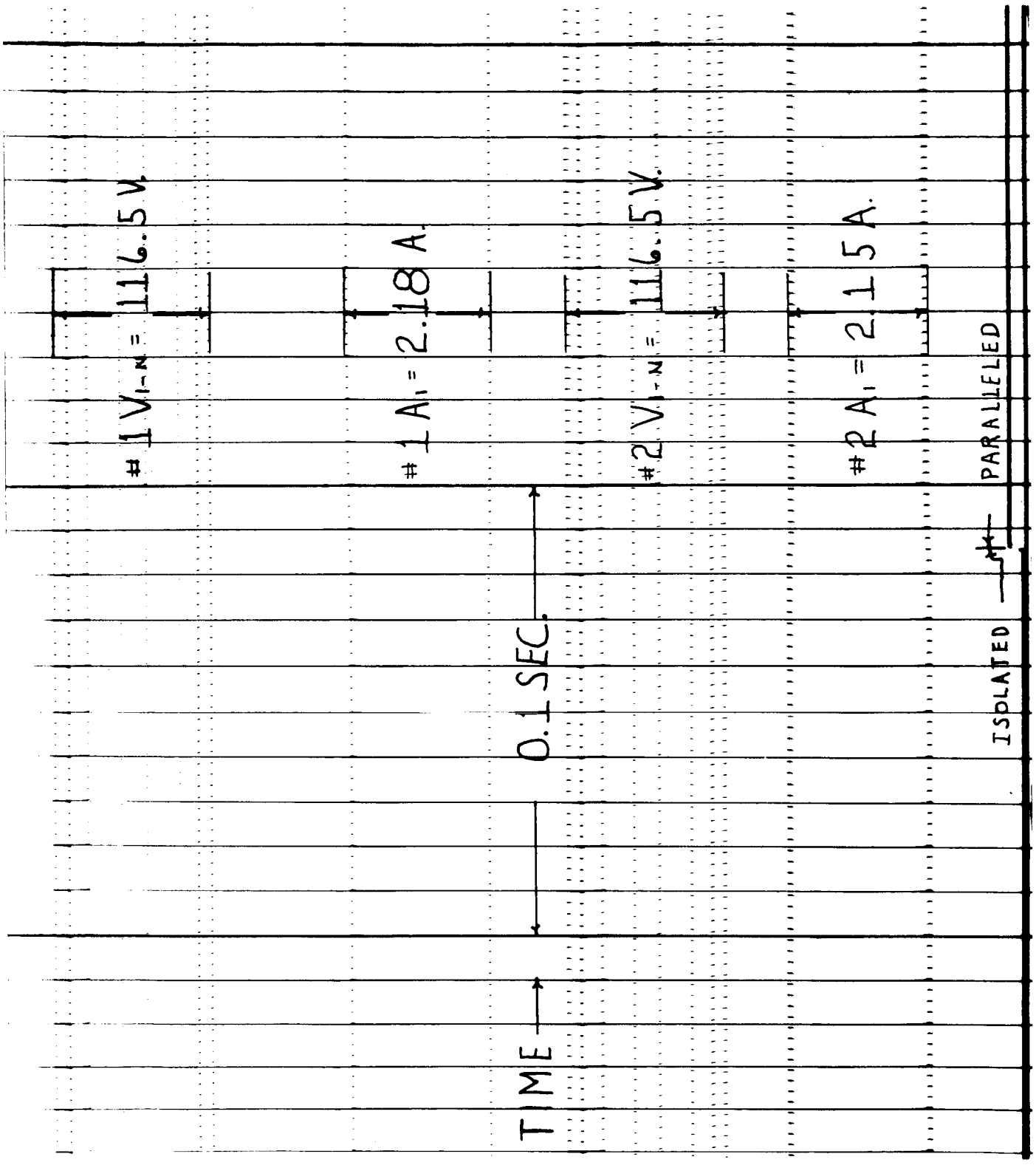

Figure 19. Oscillograph Recording of the Transient Caused by Paralleling Two Inverters. Each Inverter had a 100%, 0.75 Lagging P. F. Load on it Prior to Paralleling (Osc. #3)

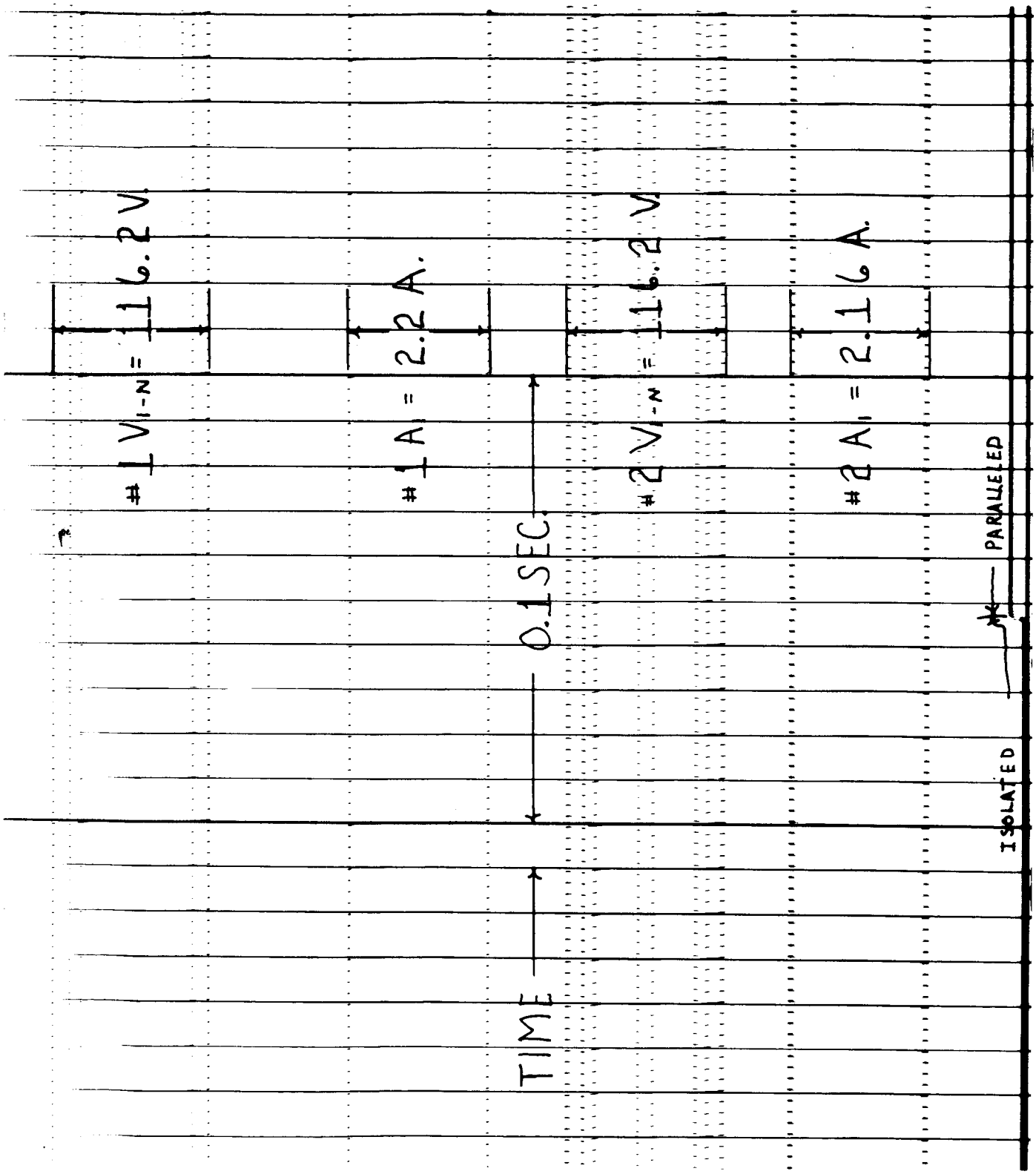

Figure 20. Oscillograph Recording of the Transient Caused by Paralleling Two Inverters. Each Inverter had a 100%, 0.9 Lagging P. F. Load on it Prior to Paralleling (Osc. #4)

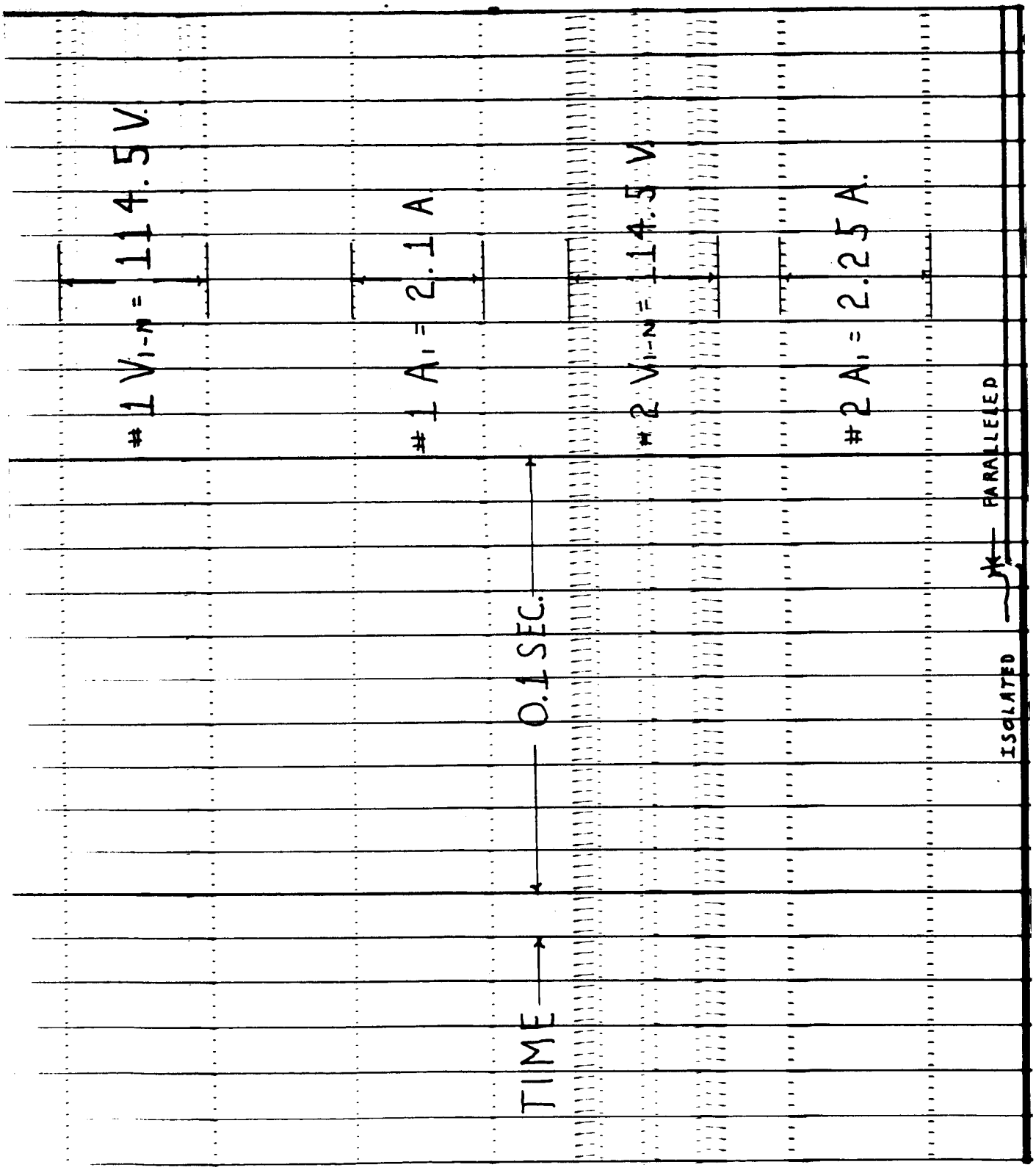

Figure 21. Oscillograph Recording of the Transient Caused by Paralleling Two Inverters. Each Inverter had a 100%, 0.9 Leading P.F. Load on it Prior to Paralleling (Osc. #5)

K 1565798

SUBJECT INVERTER/CONVERTER (P/N LYP18293 J1)

CUSTOMER ENGRG. DEPT. SERIAL NO. B.B. #1

S. O. OR TEST NO. N4-202 D. OR SPEC. NO. E2-N-5J SHAFT NO. LYP18293 FRAME NO. B.B. #2

TO DETERMINE PARALLEL INVERTER OPERATION PARA. 4.0

	PARA. 4.12			PARA. 4.13			
#1 V1-N	114.8	115					
#1 V2-N	115.	115.2		#1 V1-N	115.	114.5	
#1 V3-N	114.8	115		#1 V2-N	115	114.9	
#1 A1	2.19	1.1	OSC. #6	#1 V3-N	114	115.1	OSC. #7
#1 A2	2.18	1.09	#1 INVERTER	#1 A1	0	2.2	#1 & #2
#1 A3	2.17	1.06	WITH 100%	#1 A2	0	2.2	INVERTERS
#1 W1	253	125	1.0 PF LOAD	#1 A3	0	2.17	PARALLELED
#1 W2	253	126	AND #2 AT	#1 W1	0	252	APPLIED 2
#1 W3	250	119	NO LOAD	#1 W2	0	255	100% 1.0PF
#1 DC AMPS	38.	18.7	PARALLEL	#1 W3	0	239	LOADS AT
#1 DC VOLTS	27.7	28.8	INVERTERS	#1 DC AMPS	3.0	37.7	ONCE.
FREQ.	400	400		#1 DC VOLTS	29.8	27.7	AND
#2 V1-N	115	115		FREQ.	400	400	REMOVED
#2 V2-N	115.5	115.2		#2 V1-N	115	114.5	LOAD
#2 V3-N	114	115		#2 V2-N	115	114.9	
#2 A1	0	1.1		#2 V3-N	114	115.1	
#2 A2	0	1.1		#2 A1	0	2.15	
#2 A3	0	1.2		#2 A2	0	2.14	
#2 W1	0	128		#2 A3	0	2.3	
#2 W2	0	130		#2 W1	0	250	
#2 W3	0	135		#2 W2	0	250	
#2 DC AMPS	3.7	20.7		#2 W3	0	265	
#2 DC VOLTS	29.8	23.6		#2 DC AMPS	4.5	40.5	
FREQ.	400	400		#2 DC VOLTS	29.8	27.5	
LOAD	100%			FREQ.	400	400	
PF	1.0			LOAD	NIL	100%	
	BEFORE PARALLEL	AFTER PARALLEL		PF	—	1.0	
				THE DATA ABOVE	BEFORE LOAD ON	AFTER LOAD ON	
THE DATA ABOVE	FOR OSC. #6			FOR OSC. #7			

SEE PAGE K1565793 FOR METER DATA

SEE PAGE K1565797 FOR OSC. CALIBRATION + DATA

SEE PAGE K1563787 FOR TEST CIRCUIT SCHEMATIC

PREVIOUS TEST PAGE

3-7-64 DATE

R. MARKER - A. STEVENSON SIGNED

G. ERNS BERGER ENGINEER IN CHARGE

Figure 22. Characteristics of (Columns 1 and 2) Paralleling a Loaded Inverter with an Unloaded Inverter and (Columns 3 and 4) Parallel Inverters with Sudden Changes in Load

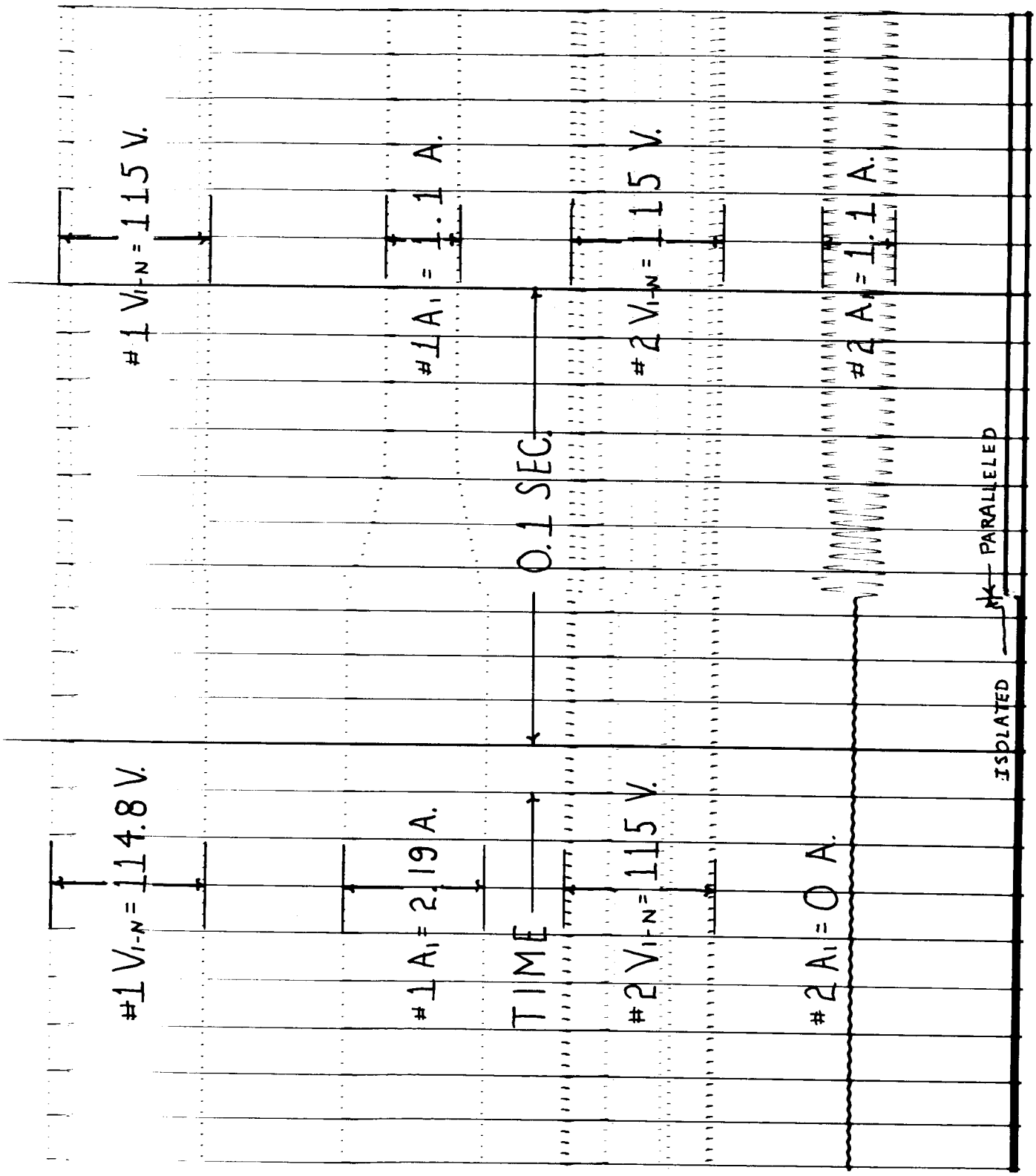

Figure 23. Oscillograph Recording of the Transient Caused by Paralleling a Loaded Inverter with an Unloaded Inverter (Osc. #6)

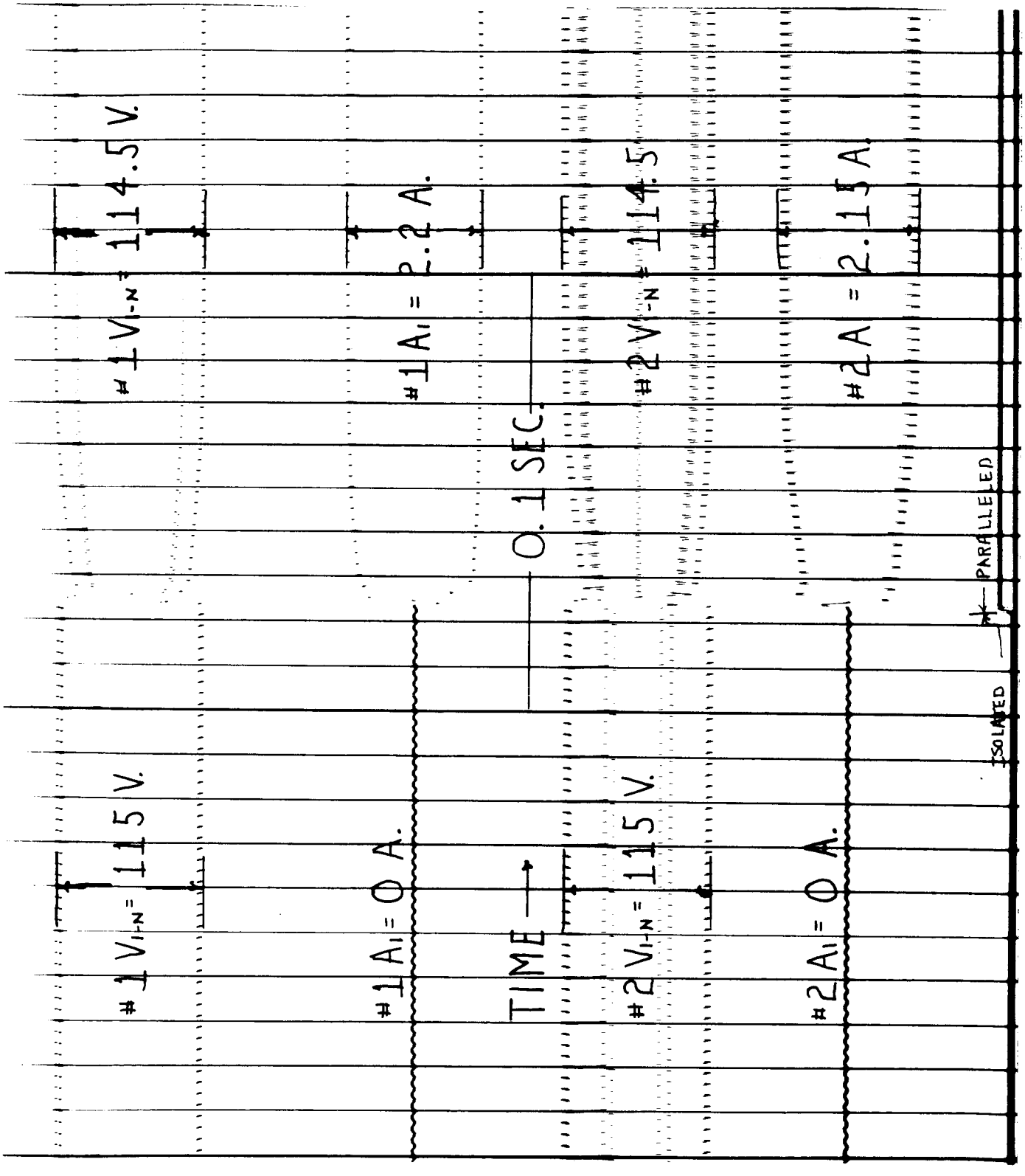

Figure 24. Oscillograph Recording of the Transient Caused by Suddenly Applying Rated Load to Two Parallel Inverters (Osc. #7)

3. Load Division With Unbalanced Three-Phase Loads.

The inverter load division tests described above include all those tests called for in the original test program. All of those tests were conducted with somewhat ideal operating conditions. Both inverter input voltages were approximately equal during the tests. Both inverter output voltages were adjusted to approximately 115 volts before paralleling. All applied loads were balanced three-phase loads. The static inverter paralleling tests described below were intentionally conducted under a variety of non-ideal conditions to determine load division circuit performance under non-ideal conditions.

The load division circuit senses the differential current of only one phase in each inverter. Figure 4 shows that phase to be phase C. Phase C current is designated as A3 on Figure 3 and on all Test Record Sheets.

It was desired to demonstrate that the paralleled inverters would share load satisfactorily under unbalanced load conditions, particularly if there were no-load on phase C. Figure 25 contains before and after paralleling data taken under four different unbalanced load conditions. Note that inverter #1 was set-up with unbalanced loads and the unloaded inverter #2 was then paralleled with it. Figures 26 through 29 are oscillograph recordings of the transients caused by paralleling the inverters. The oscillograph recordings show phase A currents and voltages for both inverters for every condition. The data show that the individual phase currents and watts are shared within 14% of rated current and watts in all cases. The worst case, as expected, occurs when phase C is unloaded.

These data illustrate a possible disadvantage of regulating the average of the three-phase voltages. The output terminal voltages under unbalanced load conditions are also unbalanced. However, as the data show, the individual phase loads can be made to share very closely without sensing all three of the phase currents. The individual phase voltages can be made to stay within a predetermined range with a predetermined amout of load unbalance by judiciously designing the output filter. Individual phase voltage regulation should be used when extremely close individual phase voltage regulation is required. This approach should be avoided if possible because it not only complicates the voltage regulation method, but it also requires that differential load currents be sensed in each output phase. This increases the complexity of the voltage regulation and load division circuits and tends to reduce the reliability of the static inverter power system.

K 166090

SUBJECT INVERTER/CONVERTER (P/N LYP 18293 J1)

CUSTOMER ENGRG. DEPT. SERIAL NO. B.B. #1

S. O. OR TEST NO. N4-202 D. OR L. SPEC. NO. E2N-5J QUALITY NO. LYP 18293 FRAME NO. B.B. #2

TO DETERMINE PARALLEL INVERTER OPERATIONS PARA 4.0

PARA. T.L. ADDITION				UNBALANCED LOADS							
	(1)			(2)			(3)			(3)	
#1 V1-N	94	108		94	104.5		126.8	120.5		131.5	125.5
#1 V2-N	118.2	118.2		112	116.5		92.8	103		96.8	107.5
#1 V3-N	132.	124.8		126.5	122.2		113	116.2		119.	119.5
#1 A1	1.87	.95		1.73	.95		0	0		0	0
#1 A2	2.24	1.15		2.1	1.11		1.72	.8		1.83	.95
#1 A3	0	0		0	0		2.13	1.1		2.24	1.1
#1 W1	182	99		118	77		0	-23		0	-11
#1 W2	266	135		178	100		120	72		179	101
#1 W3	0	-14		0	-8		130	91		265	129
#1 DC AMPS	25.4	12.3		16.2	10.4		16.5	9.0		22.7	12.2
#1 DC VOLTS	28.6	29.2		29.	29.3		28.8	29.2		28.5	29.
FREQ.	400	400		400	400		400	400		400	400
#2 V1-N	116	108		116	104.5		115.8	120.5		115.8	125.5
#2 V2-N	116	118.2		116	116.5		115.8	103		116	107.5
#2 V3-N	114.5	124.8		115	122.2		114.5	116.2		114.5	119.5
#2 A1	0	1.18		0	1.05		0	0		0	0
#2 A2	0	1.15		0	1.08		0	1.14		0	1.14
#2 A3	0	0		0	0		0	1.1		0	1.15
#2 W1	0	128		0	75		0	+23		0	+11
#2 W2	0	135		0	93		0	78		0	122
#2 W3	0	+14		0	+8		0	99		0	136
#2 DC AMPS	3.7	15.7		3.7	11.5		3.7	12.4		3.7	15.4
#2 DC VOLTS	29.7	28.9		29.7	29.2		29.5	29.		29.6	28.7
FREQ.	400	400		400	400		400	400		400	400
PF	1.0 100% LOAD ON A B C	1.0		.75 100% LOAD ON A B C	.75		.75 100% LOAD ON A B C	.75		1.0 100% LOAD ON A B C	1.0
	OSC. #8 BEFORE PARALLEL	AFTER PARALLEL		OSC. #9 BEFORE PARALLEL	AFTER PARALLEL		OSC. #10 BEFORE PARALLEL	AFTER PARALLEL		OSC. #11 BEFORE PARALLEL	AFTER PARALLEL

SEE PAGE K1565793 FOR METER DATA, K1565797 FOR OSC. CALIBRATION

SEE PAGE K1565787 FOR TEST CIRCUIT SCHEMATIC

PREVIOUS TEST PAGE 3-9-64 DATE Marber-Stevenson SIGNED G. EANSBERGER ENGINEER IN CHARGE

Figure 25. Characteristics of Parallel Inverter Operation with Unbalanced Loads

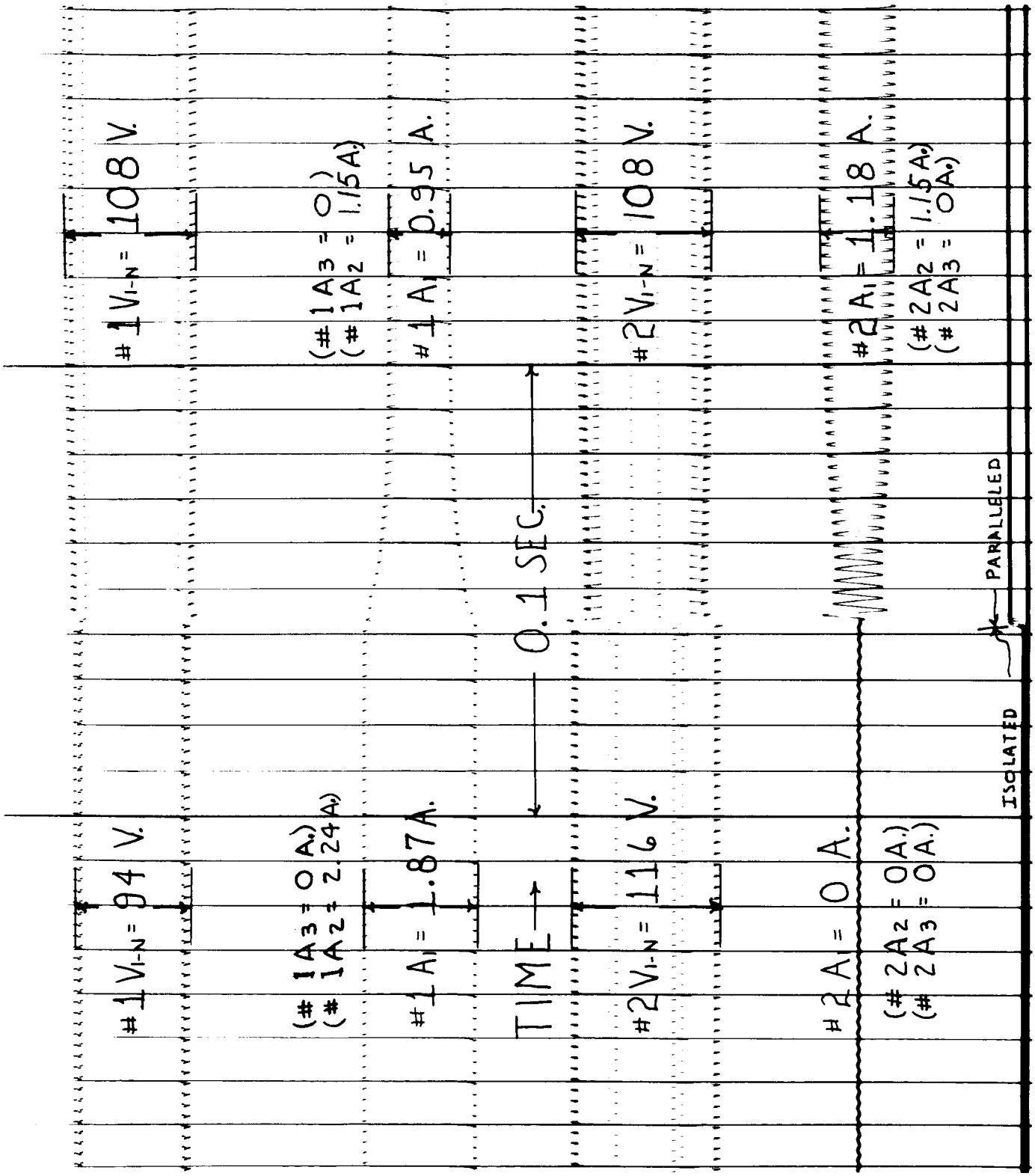

Figure 26. Oscillograph Recording of the Transient Caused by Paralleling the Inverters with Unbalanced Loads per Figure 25, Columns 1 and 2 (Osc. #8)

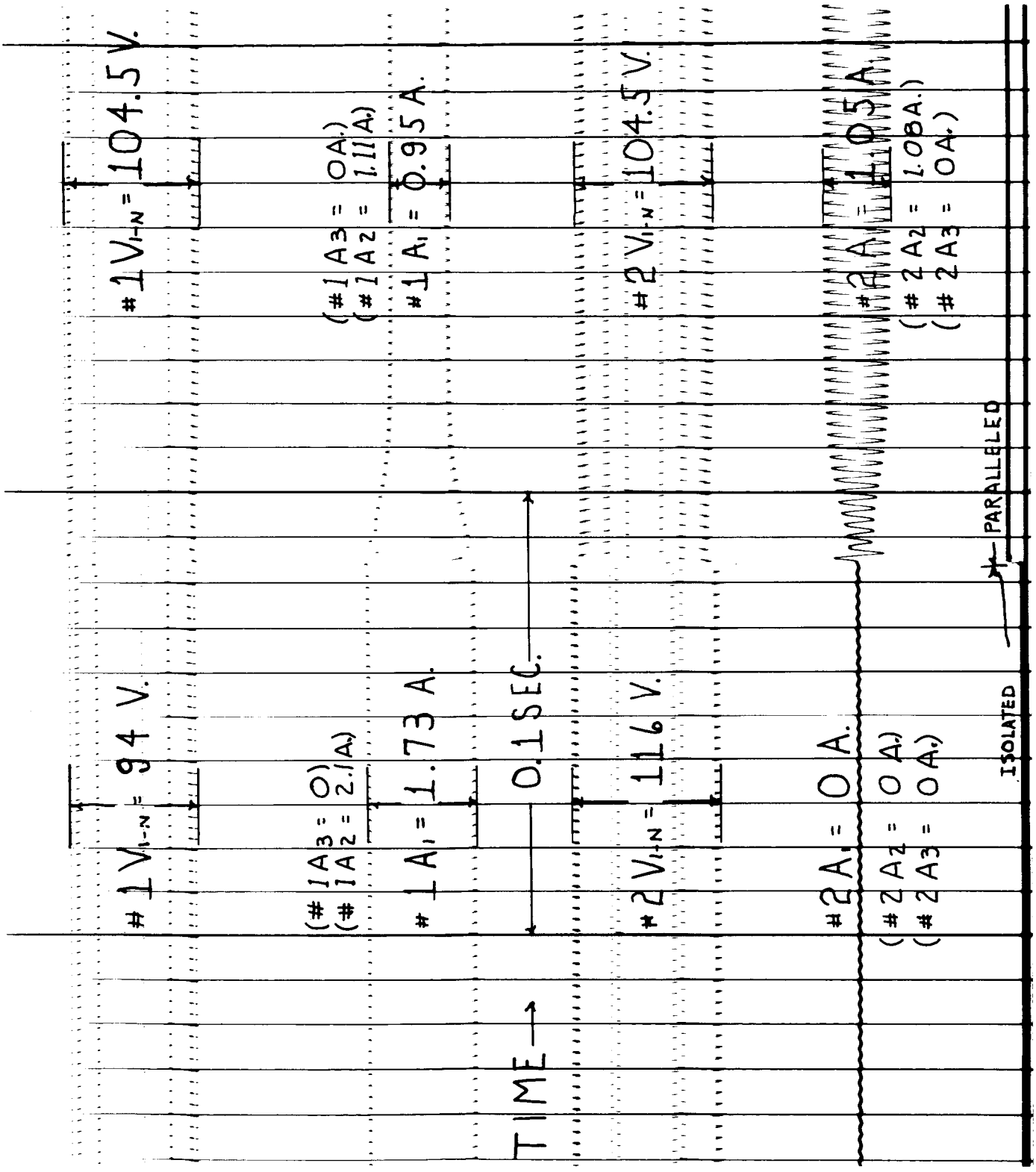

Figure 27. Oscillograph Recording of the Transient Caused by Paralleling the Inverters with Unbalanced Loads per Figure 25, Columns 3 and 4 (Osc. #9)

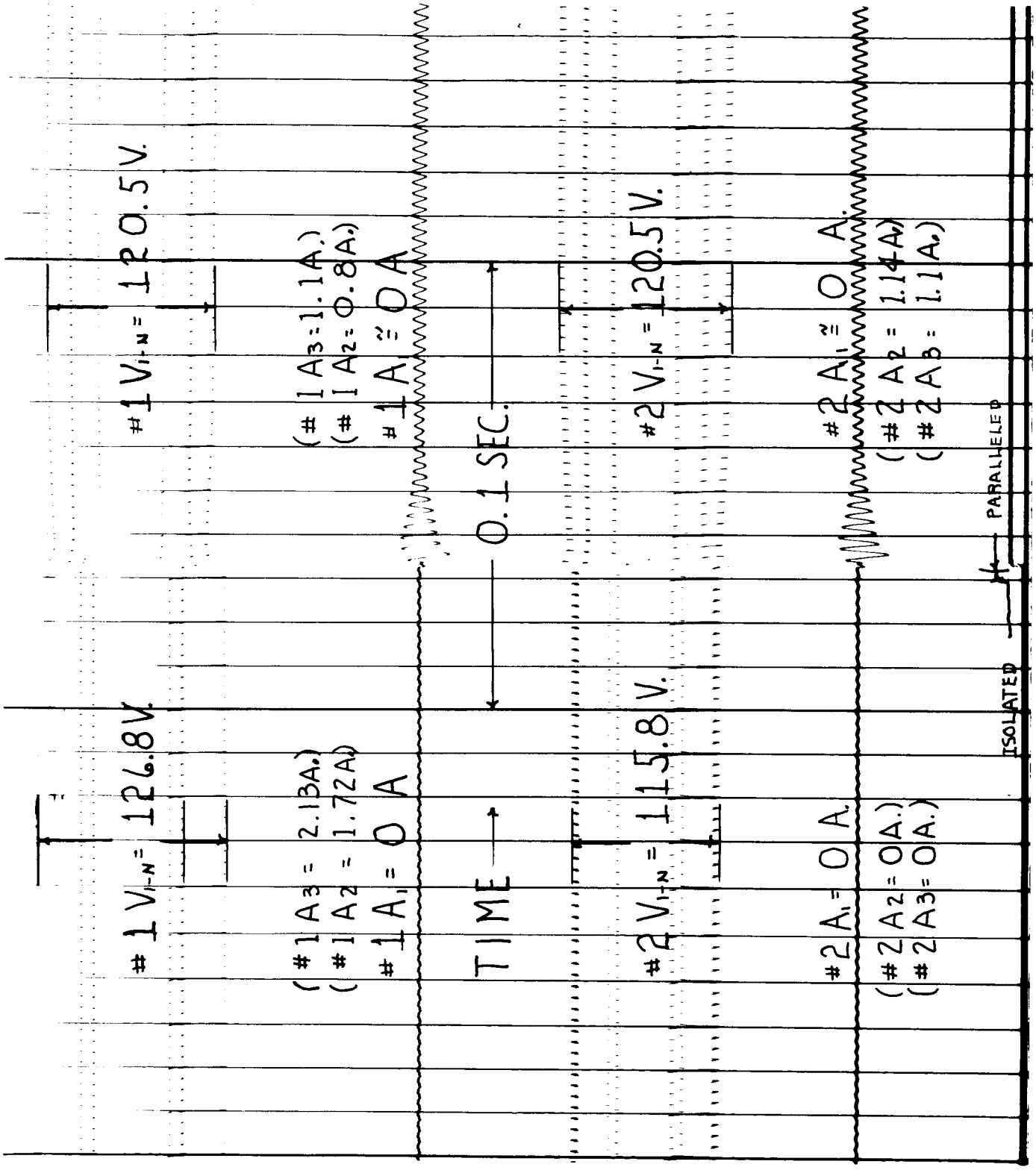

Figure 28. Oscillograph Recording of the Transient Caused by Paralleling the Inverters with Unbalanced Loads per Figure 25, Columns 5 and 6 (Osc. #10)

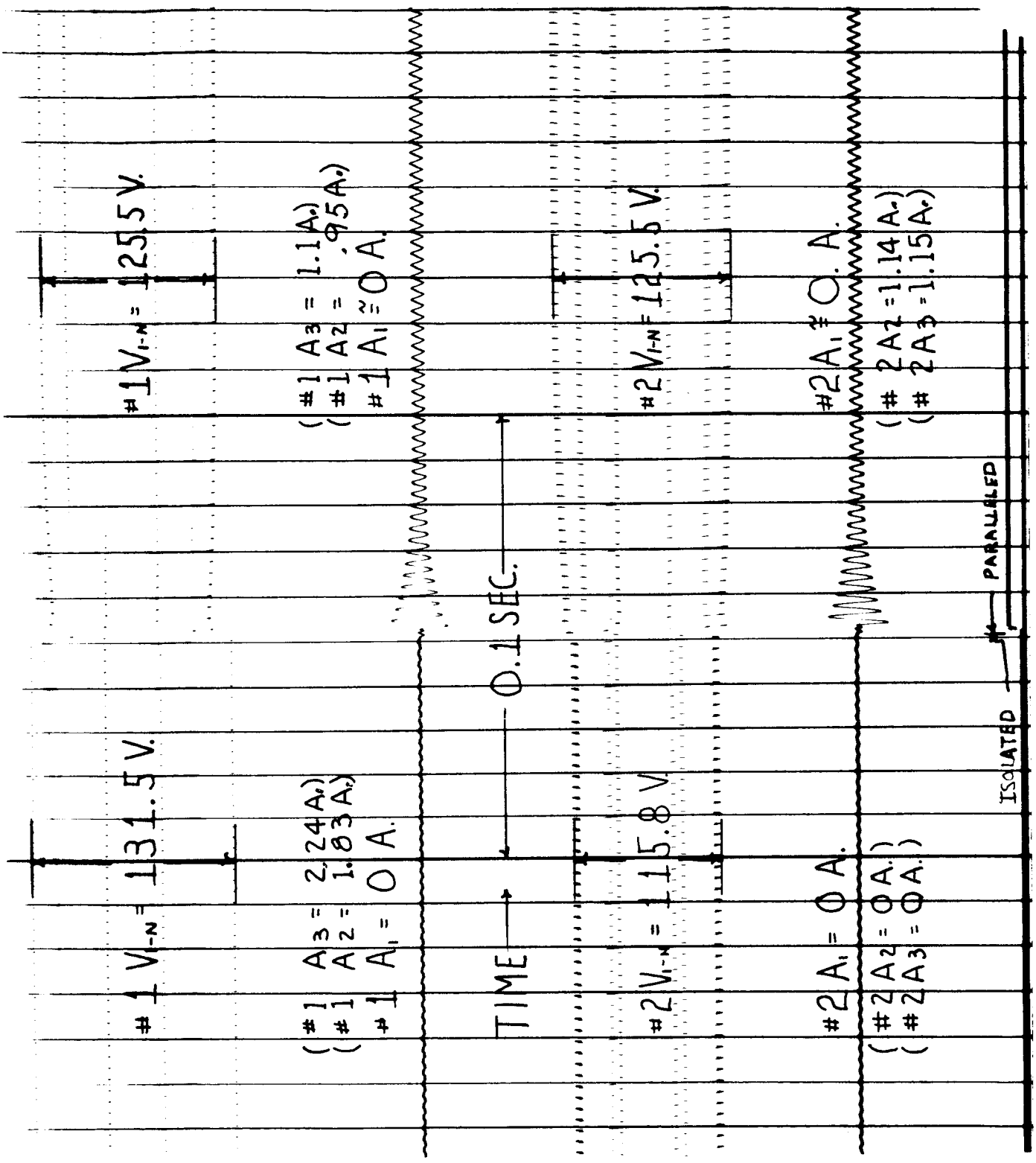

Figure 29. Oscillograph Recording of the Transient Caused by Paralleling the Inverters with Unbalanced Loads per Figure 25, Columns 7 and 8 (Osc. #11)

4. Load Division With Unequal Inverter Input Voltages.

The inverters are designed to operate with an input voltage range of 26 to 30 volts d-c. The effect on the load division circuit operation due to variation of the input voltage is shown in Figure 30. The first column contains the data taken with rated load connected to the output terminals of the unparalleled inverters with 26 volts d-c connected to the input terminals of inverter #1 and with 30 volts d-c connected to the input terminals of inverter #2. The second column contains data taken with the same condition except that the inverters are paralleled. It is obvious that input voltage variations do not appreciably affect the load division circuit operation. Figure 31 is an oscillograph recording of the paralleling transient.

5. Load Division With Unequal Inverter Output Voltages.

All previous data were taken with the terminal voltage of each inverter adjusted to an average of 115 ± 0.7 volts prior to paralleling. This was one of the criterion that was assumed during the design stage of this program. However, this condition may or may not exist in an actual application. Therefore, it was considered necessary to show that the inverters would share load reasonably well even if the terminal voltage regulating point were to drift from the ideal setting on one or both inverters. The third and fourth columns of Figure 30 contain the data taken with unbalanced regulating points.

The terminal voltage of inverter #1 was adjusted to 110 volts rms and the terminal voltage of inverter #2 was adjusted to 120 volts rms. A rated current, 1.0 pf load, was placed on inverter #1 while inverter #2 had no load on it. The data, contained in column 3, were then taken. The data of column 4 were taken after the inverters were connected in parallel. Figure 32 is an oscillograph recording of the transient caused by paralleling the inverters. Columns 5 and 6 in Figure 30 are data taken under the same conditions as were columns 3 and 4 except a 0.75 lagging pf load was used instead of the 1.0 pf load. Figure 33 is an oscillograph recording of the transient caused by paralleling the inverters with the 0.75 lagging pf load.

The loads are not shared as well as when the individual inverter terminal voltages were preset at the same voltage. However, the loads do share within 15% of the average. This performance, of course, could be improved by increasing the gain of the load division circuit.

K 1660901

SUBJECT INVERTER/CONVERTER (P/N LYP 18293 J1)

CUSTOMER ENGRG DEPT. SERIAL NO. # B.B. #1

S. O. OR TEST NO. 114-202 ~~S. OR L. SPEC. NO.~~ E2N-5J ~~SHAFT NO.~~ LYP 18293 FRAME NO. # B.B #2

TO DETERMINE PARALLEL INVERTER OPERATIONS PARA. 4.0

PARA. of T.A. ADDITION -	(1)		(2)		(1) UNBALANCED INPUT VOLTAGES ON INVERTER OUTPUT VOLTAGE ON		
					LOAD DIVISION		
#1 V1-N	115	115	110.1	115.5		110	114.5
#1 V2-N	115	114.8	110.2	115		109.8	114.
#1 V3-N	115	115	110.1	115.5		109.5	115
#1 A1	2.11	2.18	2.18	1.05		2.18	1.0
#1 A2	2.16	2.2	2.16	1.05	(3) MOTOR	2.18	.95
#1 A3	2.7	2.1	2.16	1.0	STARTING	2.15	1.0
#1 W1	251	251	242	117	CHARACTERISTICS	167	79
#1 W2	252	255	240	116	OSC.#15 START	170	86
#1 W3	241	244	238	110	½ HP MOTOR	165	77
#1 DC AMPS	40.2	40.	36.2	17.5	WITH #1 INVT.	26.5	13.1
#1 DC VOLTS	26.	26.1	28.	29.	OSC.#16 START	25.4	29.1
#1 FREQ.	400	400	400	400	½ HP MOTOR WITH	400	400
#2 V1-N	114	115	120	115.5	#1 & #2 INVT.	120	114.5
#2 V2-N	114.8	114.8	120.5	115	PARALLELED	120	114
#2 V3-N	114.1	115	1.7	115.5	MOTOR (W)	119	115
#2 A-1	2.19	2.16	0	1.25	P/N 35A9097-2	0	1.3
#2 A-2	2.15	2.15	0	1.23		0	1.34
#2 A-3	2.16	2.17	0	1.3		0	1.34
#2 W-1	254	251	0	145		0	105
#2 W-2	254	250	0	147		0	100
#2 W-3	252	252	0	155		0	107
#2 DC AMPS	39.1	24.1	4.0	23.0		4.0	18.0
#2 DC VOLTS	30	[illegible]	29.7	25.6		29.7	28.5
#2 FREQ.	400	[illegible]	400	400		400	400
LOAD	100%		100%			100%	
PF	1.0		1.0			.75	
OSC.	#12 BEFORE PARALLEL	AFTER	OSC. #13 BEFORE PARALLEL	AFTER		OSC. #14 BEFORE PARALLEL	AFTER

SEE PAGE K 1565793 FOR METER DATA, K1565797 FOR OSC. CALIBRATION
SEE PAGE K 1565787 FOR TEST CIRCUIT SCHEMATIC

PREVIOUS TEST PAGE

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DATE SIGNED ENGINEER IN CHARGE

Figure 30. Miscellaneous Test Data

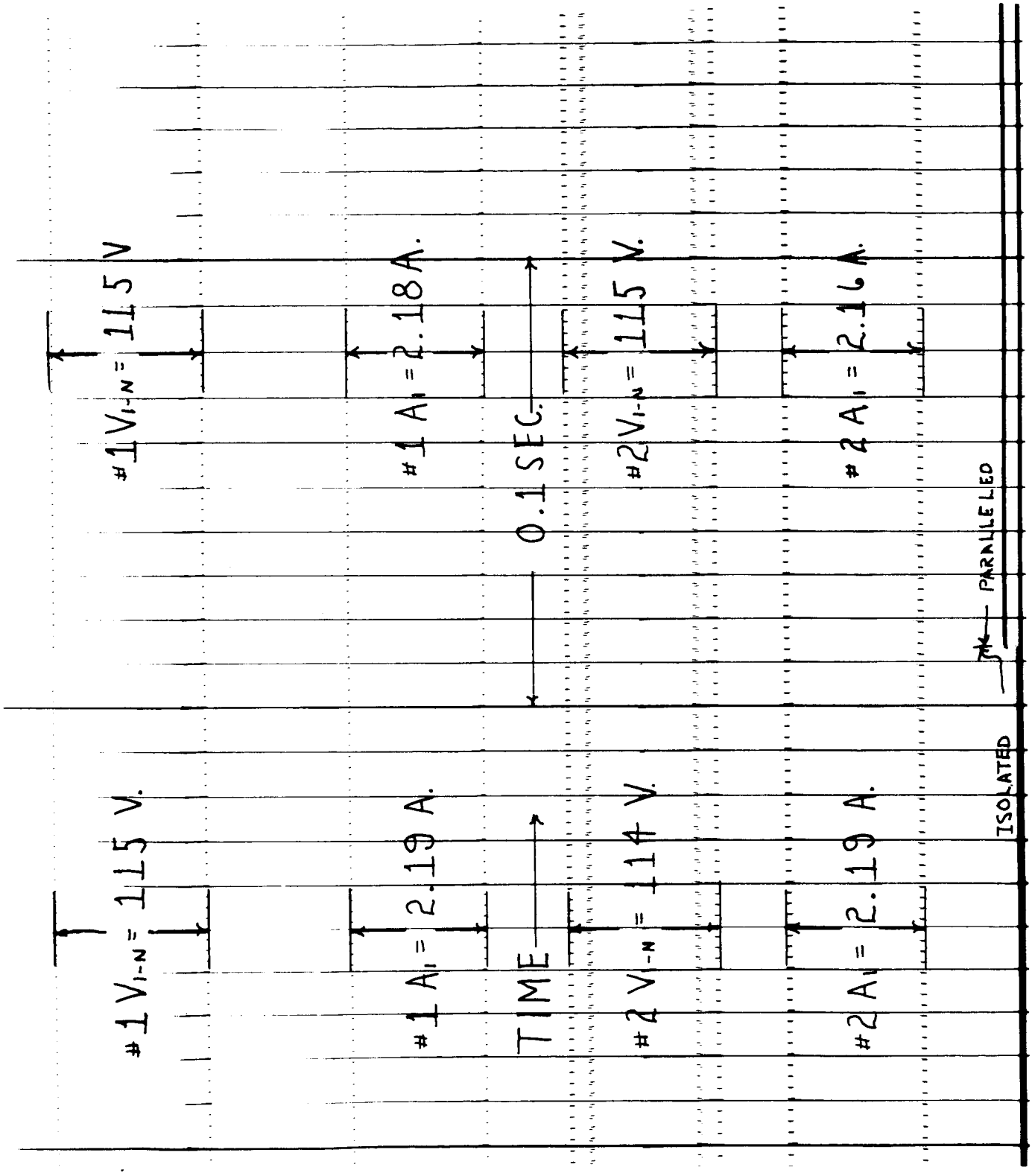

Figure 31. Oscillograph Recording of the Transient Caused by Paralleling the Inverters with Unequal Input Voltages (Osc. #12)

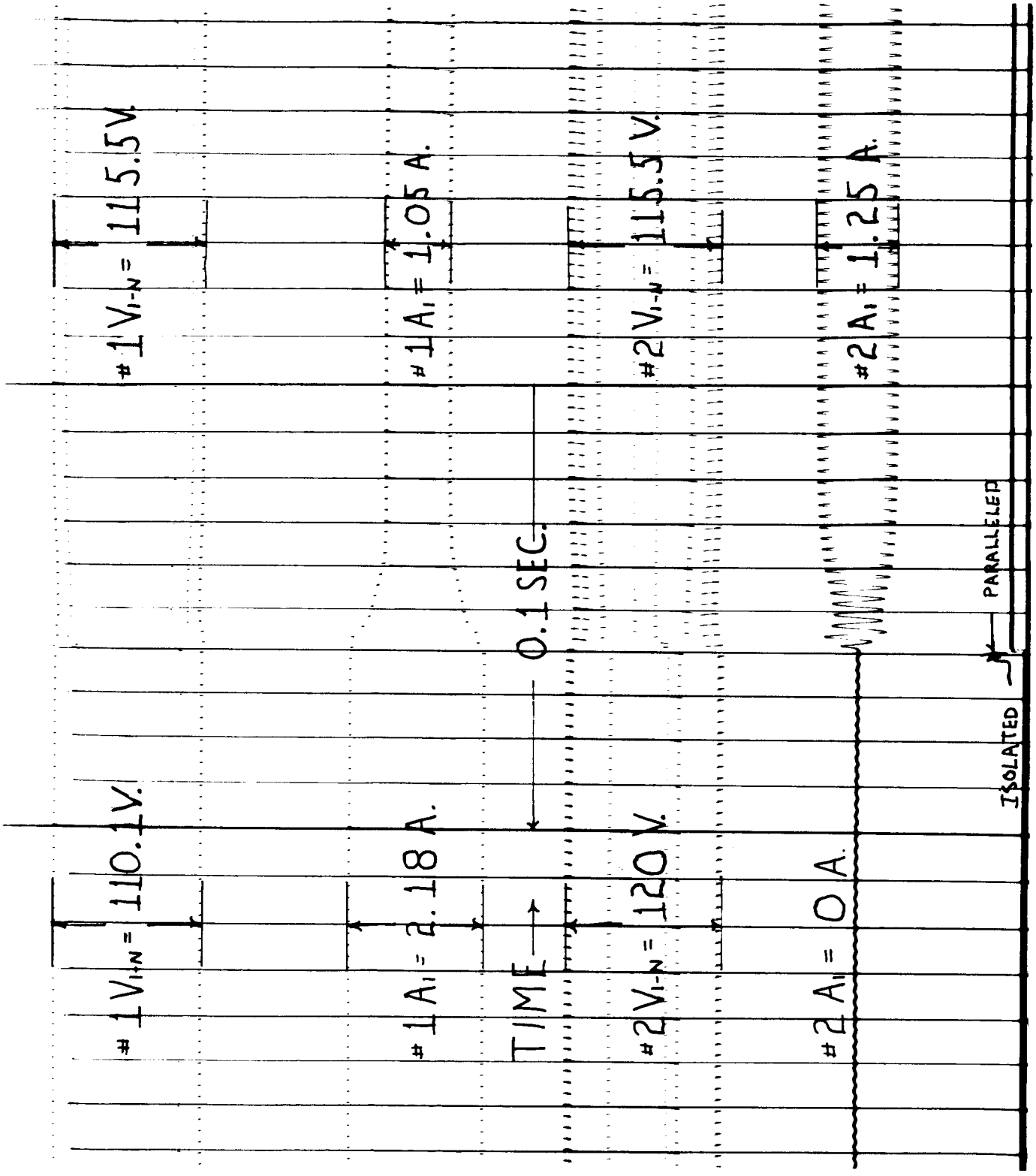

Figure 32. Oscillograph Recording of the Transient Caused by Paralleling the Inverters with Initially Unequal Output Terminal Voltages. Load is 1.0 P. F., Rated Current for One Inverter (Osc. #13)

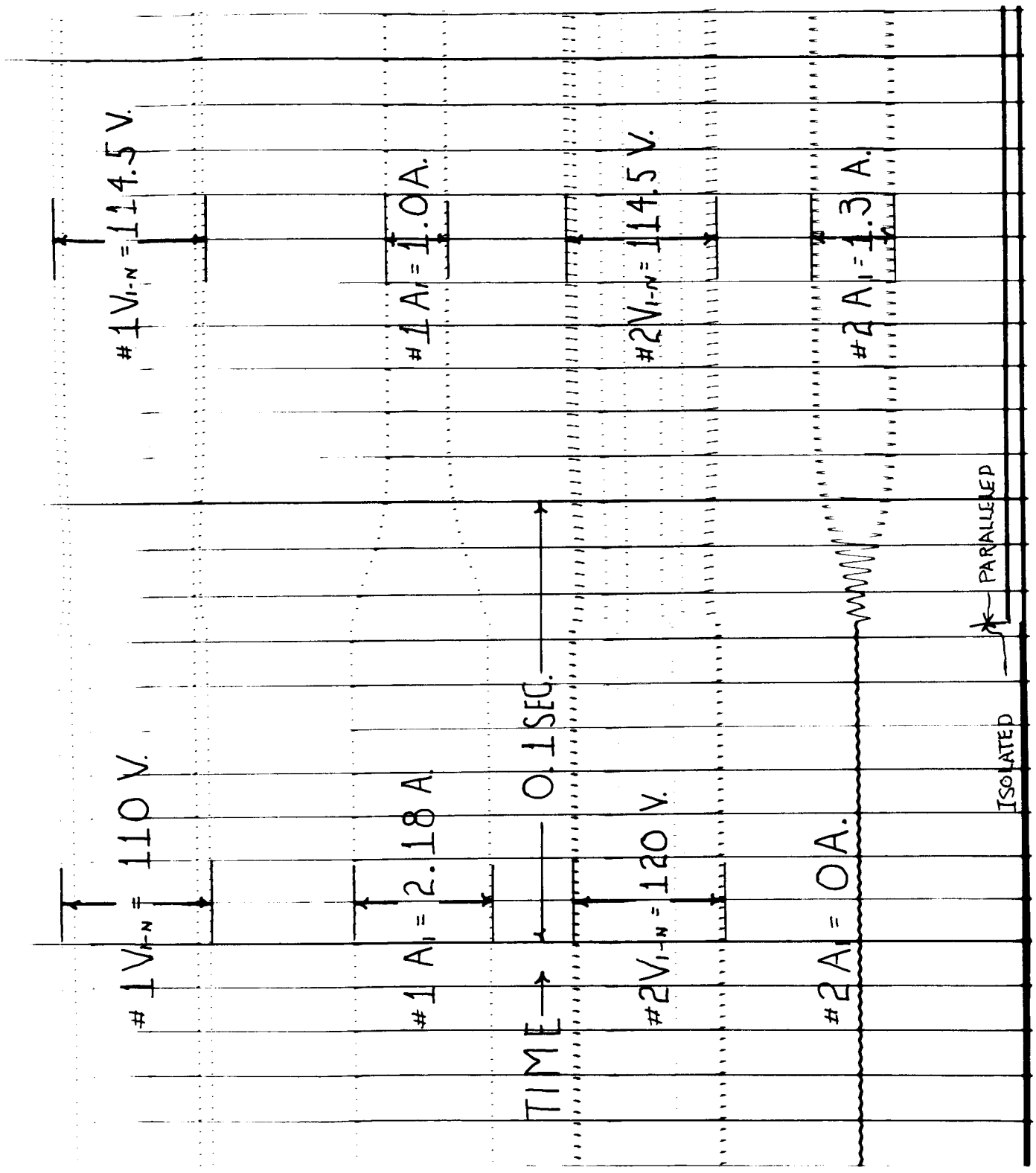

Figure 33. Oscillograph Recording of the Transient Caused by Paralleling the Inverters with Initially Unequal Output Terminal Voltages. Load is 0.75 Lagging P.F., Rated Current for One Inverter (Osc. #14)

6. Load Division While Starting an Induction Motor.

Figure 34 is an oscillograph recording showing a 1/8 HP induction motor starting current transient being supplied by inverter #1. Figure 35 is an oscillograph recording showing the motor starting current being supplied by the two inverters connected in parallel. Note that the parallel inverters share current during the starting transient. This shows that a motor which requires more starting current than one inverter can supply can be started with two or more inverters connected in parallel.

D. Experimental Determination of Static Inverter Internal Impedance.

The internal impedance of the static inverter was determined analytically in the first quarterly report. The internal impedance was found to be:

$$\dot{Z}_1 \cong 0.27 \text{ P.U. } \underline{/77.8^\circ}.$$

The actual internal impedance of the static inverter breadboard was determined experimentally to be:

$$\dot{Z}_1 = 0.305 \text{ P.U. } \underline{/70.3^\circ}$$

which is in reasonably close agreement with the originally calculated value above.

The procedure used to measure the internal impedance is described in Appendix II. Because of the relative ease of measuring the internal impedance of a static inverter, this procedure is preferred to the calculation method described in the first quarterly report and should be used whenever an inverter model is available for the purpose.

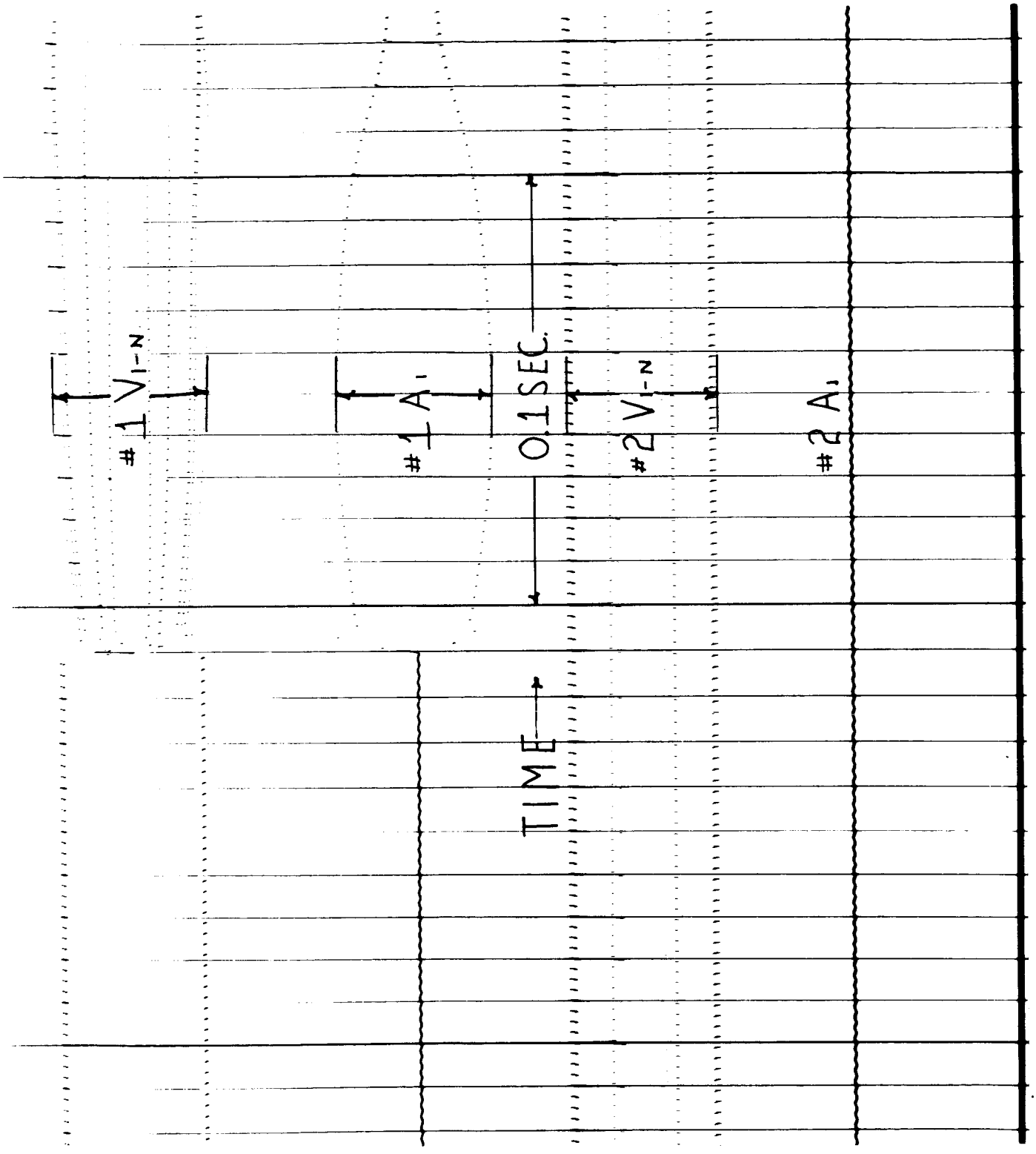

Figure 34. Oscillograph Recording of One Inverter Starting a 1/8 H. P. Motor (Osc. #15)

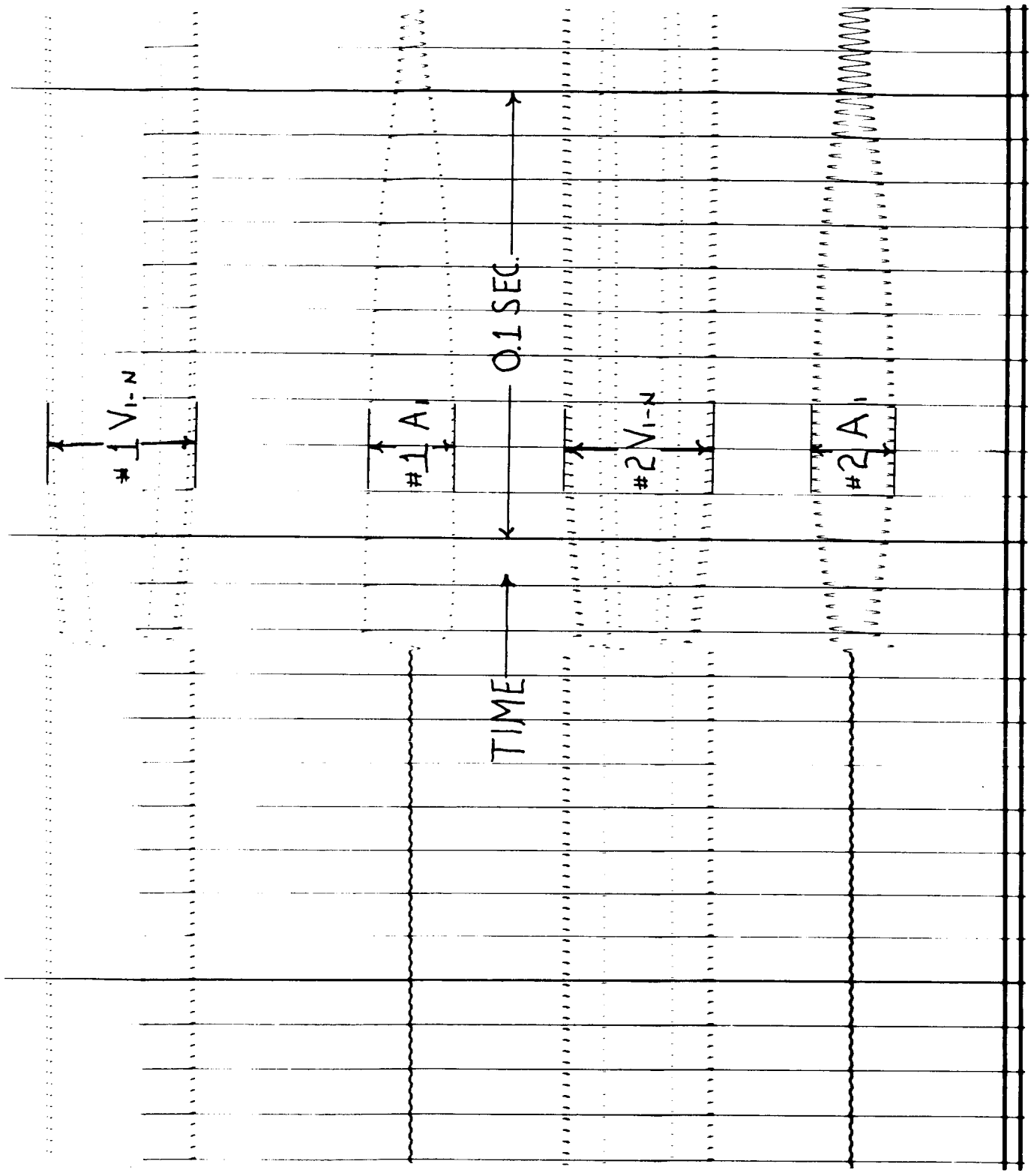

Figure 35. Oscillograph Recording of Two Parallel Inverters Starting a 1/8 H. P. Motor (Osc. #16)

III. STATIC CONVERTER PARALLELING EVALUATION

A. Single Converter Operation Test.

Terminal board interconnections were made on each inverter/converter model in accordance with Figure 10 of the Second Quarterly Report (Figure 75 of this report). This changes the static inverter output from wye to delta and connects this output to a three-phase full-wave rectifier. The output of the rectifier is considered the output of the static converter model. This d-c output voltage was connected to the same zener voltage reference and voltage regulator circuit that was used for the static inverter. By adjusting resistor R15, the converter output voltage was set to regulate at the rated converter output voltage, 153.5 volts d-c.

The converter output current was caused to pass through a transductor which was designed to produce a d-c output voltage proportional to the converter d-c output current. The transductor output voltage appears across a variable resistor, R69. This variable resistor was set in each static converter model by applying rated load (4.88 amperes d-c) to each converter and adjusting resistor R69 until 20 volts d-c was measured across it. The transductor operating characteristics were recorded for each model from 0 to 6 amperes. This data is recorded in Figures 36 and 37 for converter model #1 and #2 respectively and is plotted in Figure 38. Figure 38 shows the good linearity and repeatability which can be obtained from these simple-saturable-reactor circuits. This linearity and repeatability is necessary to obtain good current division between or among converters over wide load ranges.

B. Load Division Circuit Modification.

When the two converters were connected in parallel, the load current was not shared equally between converters as planned. Instead, all of the load current was supplied by whichever converter had the highest output voltage. The load division circuit had no effect at all on the division of load. By careful examination of the converter load division method, described in the first quarterly report, the reason for the poor load division was determined and has been corrected by circuit modification.

The original converter load division circuit is shown in Figures 14 and 27 of the first quarterly report. For converter operation, the zener diode voltage reference (CR55, CR56, R18, R19, R15, R68) is connected to the converter output voltage by a jumper wire from "S3" to "+ output". The output of this bridge type voltage detector acts through R17 and a control winding of the magnetic-amplifier in the voltage booster to maintain the converter output voltage at a level predetermined by the setting of resistor R15. This voltage regulator circuit must

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SUBJECT INVERTER/CONVERTER MODEL 4N LYP18293 J1 SERIAL NO. C.E. #1

CUSTOMER ENGINEERING DEPT.

S. O. OR TEST NO. N4-202 D. OR L. SPEC. NO. E2N-5J SHAFT NO. LYP18293 FRAME NO.

TO DETERMINE OPERATING CHARACTISTICS OF CONVERTER TRANSDUCTOR (130)

PARA 5.0 SINGLE CONVERTER OPERATION TEST

PARA 5.5
-L.C. OUTPUT VOLTAGE SET AT 153.5 VOLTS
BY ADJUSTING R15

PARA 5.6
VOLTAGE ACROSS R69 ADJUST TO 20.0 VOLTS DC.
L.C. OUTPUT CURRENT 1.88 AMPS.

PARA 5.7

CONVERTER OUTPUT CURRENT	DC VOLTAGE ACROSS R69
0 AMPS.	.12 VOLTS.
.61	3.05
1.0	4.66
2.0	8.6
3.	12.3
4.0	16.2
5.6	20.3
6.0	23.5

R61 = 1161 Ω OHMS

METERS USED:

DC VOLTS	(W)	MODEL Px5	S/N 1517824	C.K	300
DC AMPS	(W)	MODEL Px5	S/N 2600416	C.K	10
DC VOLTS	(R61) TRIPLETT	MODEL 630	S/N 149739	C.K	3-12-60

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FEB 26 1964 DATE

W. MILLER SIGNED

G.W. FUNSTEN ENGINEER IN CHARGE

Figure 36. Unfiltered Operating Characteristics of Converter #1 Transductor

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SUBJECT: Inverter/Converter Model P/N LYP 18293 J1

CUSTOMER: Engineering Dept

SERIAL NO.: BB #2

S. O. OR TEST NO.: N4-202 D. OR L. SPEC. NO.: E2N-5J SHAFT NO.: LYP 18293 FRAME NO.:

TO DETERMINE: Operating Charactistics Of Converter Transductor (T30)

Para 5.0 Single Converter Operation Test.

Para 5.5
D.C Output Voltage Set At 153.5 Volts
By Adjusting R15

Para 5.6
Voltage Across R69 Adjust To 20.0 Volts D.C.
D.C. Output Current 4.88 Amps.

Para 5.7

Converter DC Output Current	D.C. Voltage Across R69
0 Amps	.99 Volts
.6	2.42
1.0	4.1
2.0	8.4
3.0	12.4
4.0	16.7
5.0	20.7
6.0	23.6

R69 = 1135 Ω Ohms

Meters Used;

DC Volts	(W)	Model PX5	S/N 1517824	C-R 300
DC Amps	(W)	Model PX5	S/N 260046	C-R 10
DC Volts	(R69) Triplett	Model 630	S/N 149739	C-R 3-12-60

PREVIOUS TEST PAGE

DATE: Feb 26, 1964 SIGNED: W Miller, H. W. K. Ridenour ENGINEER IN CHARGE: G.W. Ernsberger

Figure 37. Unfiltered Operating Characteristics of Converter #2 Transductor

The second load division method was actually incorporated in the two model converters and is shown schematically in Figures 4 and 39. This method uses the same transductor and voltage detector that were designed for the original load division method but, only one magnetic-amplifier control winding is required. Figure 39 will be used to describe the operation of the modified load division circuit and shows two converters connected in parallel. The converter operation and voltage regulation method are unchanged and have been previously described. The only change in the voltage sensing circuit is that voltage dropping resistors, R68 and R15, have been connected to the negative output terminal rather than the positive output terminal. The transductor circuit remains unchanged except for the addition of a filter capacitor, C21, across its output. This capacitor and a converter output filter, L6 and C22, were found necessary to prevent low frequency modulation of the individual converter load currents during parallel operation. When CONVERTER A LOAD CURRENT equals CONVERTER B LOAD CURRENT, the transductor outputs across R69A and R69B are equal. During this condition, there is no potential difference to cause a current to flow in the Y1 circuit. If CONVERTER B LOAD CURRENT exceeds CONVERTER A LOAD CURRENT, then the voltage across R69B exceeds the voltage across R69A and a current, I_{Y1}, will flow in the direction shown. This current reduces the voltage drop across R68B and R15B which increases the voltage across the voltage detector bridge: R18B, R19B, CR55, and CR56. The unbalanced bridge causes a current to flow in the magnetic-amplifier control winding in the direction shown; this control current causes the associated voltage-booster to reduce the d-c voltage applied to INVERTER B which causes CONVERTER B LOAD CURRENT to decrease. The polarity of I_{Y1} shown, causes the opposite effect in CONVERTER A LOAD CURRENT. These effects together tend to cause the converter load currents to remain nearly equal. Any number of similar converters may be connected in parallel by this method.

The gain required of the converter load division circuit to assure that a given converter will supply no more than 10% above or below the average converter output current was determined on page 38 of the first quarterly report to be:

$$\frac{\partial E}{\partial I_{DR}} = 0.244 \frac{\text{P.U. d-c volts}}{\text{P.U. d-c unbalanced current}}$$

The gain required is inversely proportional to the permitted load unbalance. The load division circuit modification decreased the gain of the circuit. The new load division circuit gain will be calculated below.

The converter internal voltage, E, (i.e., the no-load output voltage) will change an amount equal to the voltage across resistors R68 and R15 which is caused by current I_{Y1}. The transductor output voltage can be considered a voltage source with an internal impedance of R69. The transductor output voltage is related to the converter output current by the following ratio:

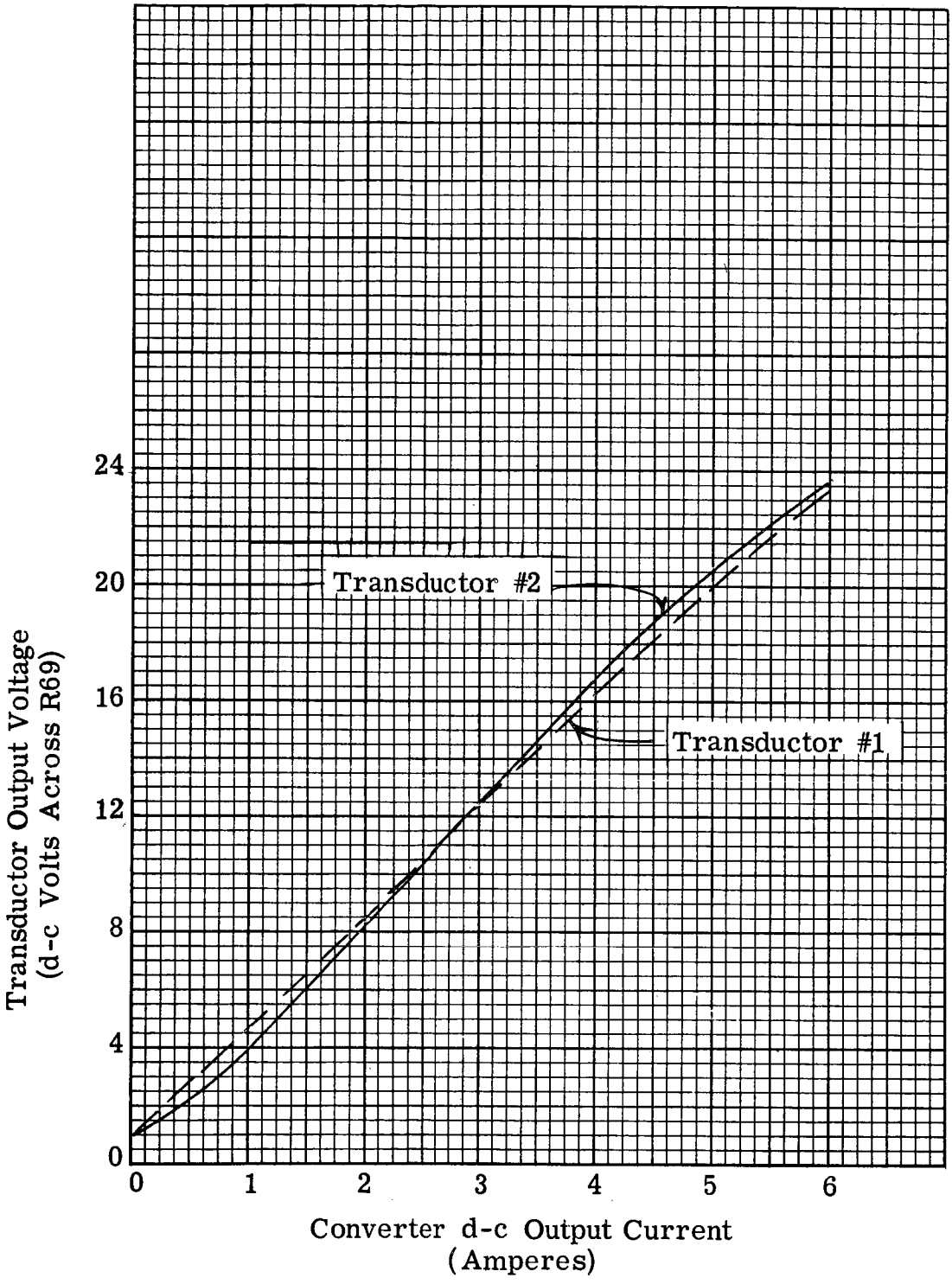

Figure 38. Linearity of Transductor Unfiltered Output Voltage

have high gain to maintain good output voltage regulation. The required voltage regulator gain, $\frac{\partial E}{\partial V_S}$, was determined (see pages 36 and 37 in first quarterly report) to be -22.87 to limit the no-load to full-load voltage droop to 0.0061 P.U. volts. This gain means that if the converter is operated "open loop", (i.e., the output voltage sensing circuit is disconnected from the converter output terminals) a one-volt increase in sensing voltage will decrease the converter output voltage 22.87 volts.

The original converter load division circuit was designed to have a gain, $\frac{\partial E}{\partial I_{DR}}$, of 0.244 $\frac{\text{P.U. d-c volts}}{\text{P.U. d-c unbalanced current}}$. The converter load division circuit output acts through a second control winding on the same magnetic-amplifier and has this gain when the output voltage sensing circuit is inoperative. However, when the output voltage sensing circuit is operating and maintaining the converter output voltage at 153.5 volts, then the converter load division circuit has practically no effect on the converter output voltage. The small current, which the load division circuit passes through the second control winding on the magnetic amplifier, is cancelled out by control current from the output voltage sensing circuit. Therefore, when one converter output voltage was set at 154 volts and the other converter was set at 153 volts, before paralleling, the output voltage of both converters would be 154 volts, after paralleling. This output voltage is one volt too high for the converter that had been set to regulate at 153 volts. Its voltage sensing circuit causes its booster voltage to decrease and that converter supplies no part of the load current. This condition would continue until an increasing load caused the output voltage to decrease to 153 volts or less.

At least two methods are available to correct this unacceptable load division circuit. One method, currently being used on regulated a-c to d-c converters, uses three control windings on the magnetic amplifier. 1) One winding has a relatively large constant d-c current through it, usually derived with a resistor from a constant voltage source. This control current polarity tends to increase the converter output voltage. 2) A second winding has a relatively large d-c current through it which is proportional to the converter output voltage. This control current polarity is opposite of the first winding and is adjusted so that the converter output voltage is at the desired level. 3) The third control winding is connected in the same manner as winding R2-L2 in the original load division circuit. Current in this winding must be proportional to the differential load current. The polarity of this winding must be such that the converter output voltage tends to increase when the converter is supplying less than the average of all converter output currents and vice versa. This is an acceptable converter load division method for applications where close voltage regulation limits are not required over wide temperature ranges. For good voltage regulation with this method, the magnetic-amplifier characteristics must remain essentially unchanged for all operating temperatures. This method was not considered further because of this inherent application restriction.

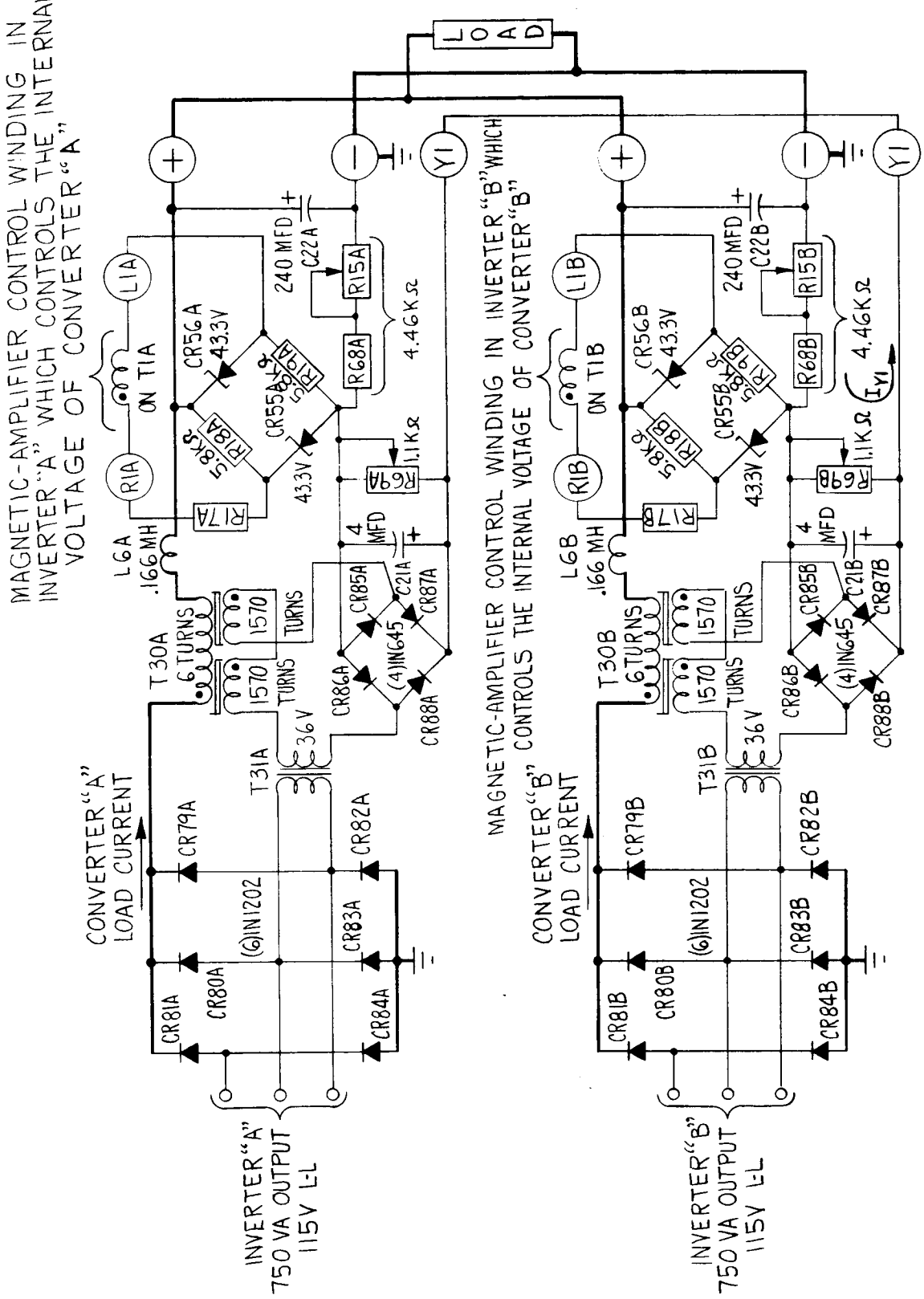

Figure 39. Schematic Diagram of the Modified Converter Load Division Circuit

$$\frac{\text{Transductor output volts}}{\text{Converter load current}} = \frac{20 \text{ volts}}{4.88 \text{ amps}}$$

If converter B output current exceeds the average converter output current, the difference between transductor B output voltage and the average transductor output voltage will be proportional to the differential current I_{DR}. The portion of the differential transductor output voltage which affects the voltage across resistors R68 and R15 is determined by the ratio of R68 + R15 to R68 + R15 + R69. The modified load division circuit gain is therefore:

$$\frac{\partial E}{\partial I_{DR}} = \frac{\text{Transductor output volts}}{\text{Converter load current}} \times \frac{R68 + R15}{R68 + R15 + R69}$$

$$= \frac{20 \text{ volts}}{4.88 \text{ amps}} \times \frac{4.46K}{5.56K}$$

$$= 3.28 \frac{\text{converter d-c volts change}}{\text{d-c amperes unbalanced current}}$$

This gain calculated in per-unit values is:

$$\frac{\partial E}{\partial I_{DR}} = 3.28 \times \frac{1 \text{ P.U. d-c volts}}{153.5 \text{ d-c volts}} \times \frac{4.88 \text{ d-c amperes}}{1 \text{ P.U. d-c amperes}}$$

$$= 0.105 \frac{\text{P.U. d-c volts}}{\text{P.U. d-c unbalanced current}}$$

This modified load division circuit gain can be expected to limit the load unbalance to:

$$10\% \times \frac{0.244}{0.105} = 23.2\%$$

This is not a close limit for a load division circuit. However, from the derivation of this gain, it is apparent that the load division circuit can be designed to have any desired gain for any desired load division limit. The load division circuit gain can be increased by increasing the rated transductor output voltage. Actual test results of this modified load division circuit are given in the next section.

C. Load Division Circuit Evaluation.

To evaluate the parallel performance of the modified load division circuit, the two static converter models were interconnected in the laboratory as shown in Figure 40. The meters and load resistors used for this test are shown in the left foreground of Figure 40 and are shown schematically in Figure 41.

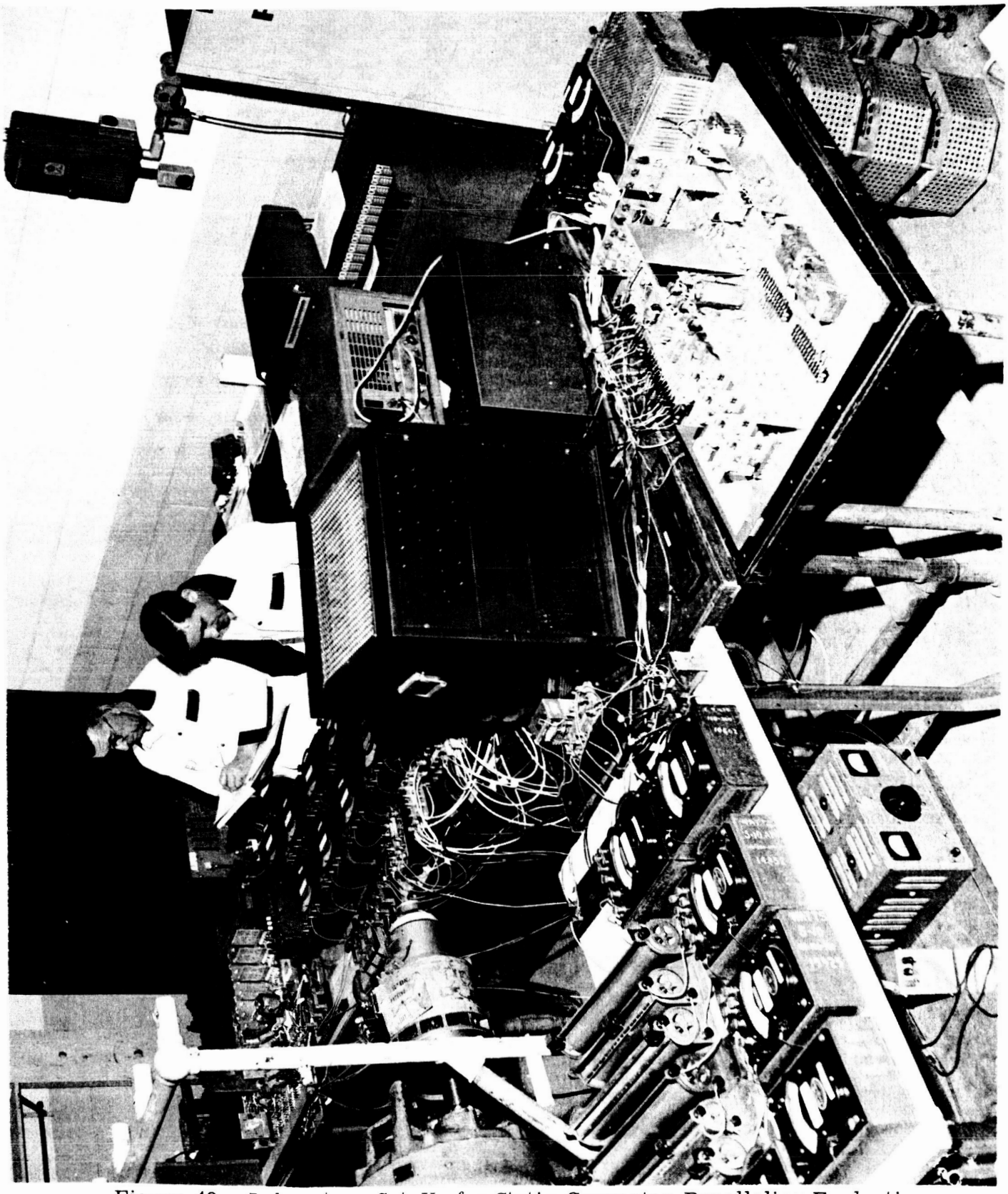

Figure 40. Laboratory Set-Up for Static Converter Paralleling Evaluation

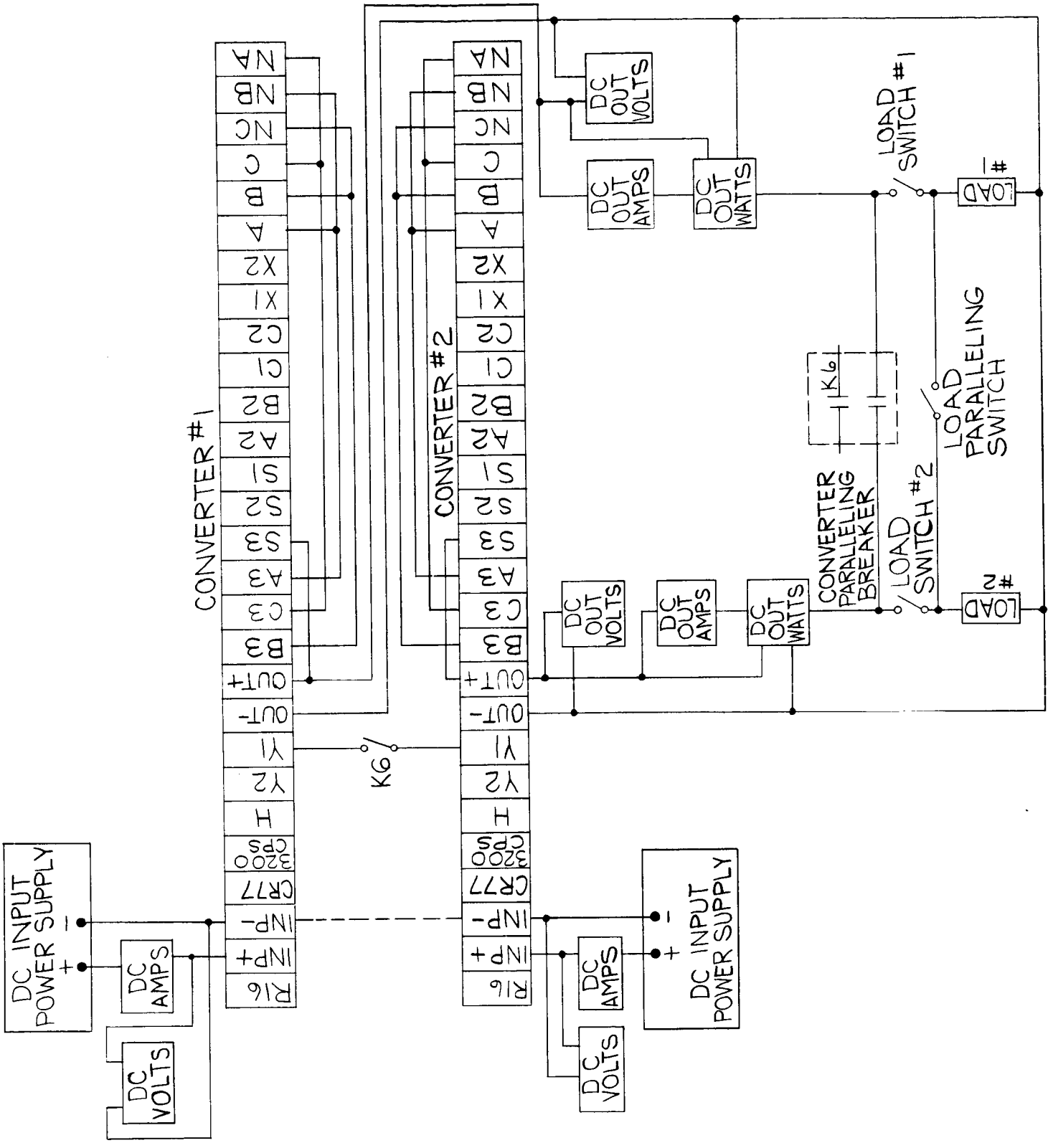

Figure 41. Schematic Diagram Showing Interconnection of Converter Models for Parallel Performance Evaluation

The transductor operating characteristics were measured again. Test results are given in Figure 42 with a four microfarad capacitor added across R69. The addition of this filter capacitor across the transductor output required a small adjustment of R69 but the operating characteristics are essentially the same as shown in Figure 38.

When the two converters were connected in parallel, load current was shared better than expected. The requirements for paralleling converters are simple compared to paralleling inverters. The converter output voltages must be nearly the same before paralleling. The Y1 terminals must be connected together at the same instant the converter output terminals are connected in parallel. For the initial paralleling evaluation, each converter output voltage was set at 153.5 volts, no-load, prior to paralleling. After paralleling, load division was determined for 0, 25, 50, 75, 100, and 125% loads. These test results are recorded in Figure 43. Oscillograph recordings were made of both converter output voltages and currents during the paralleling operations. Figures 44 and 45 are calibration traces taken during isolated operation. Figures 46 through 51 are oscillograph recordings made during the paralleling operations with from zero to 125% rated load on each converter prior to paralleling.

To demonstrate that an unloaded converter can be paralleled with a fully loaded converter, data were recorded under these conditions on Figure 52. Figure 53 is an oscillograph recording of this paralleling transient. The load current unbalance between converters was 3.4% after paralleling.

To demonstrate that large load transients can be sustained by the paralleled converters, the unloaded converters were connected in parallel. A 100% rated load was then applied simultaneously to both converters. The successful test results are recorded in Figure 52. Figure 54 is the oscillograph recording of this load transient.

Identical regulated static converters will share load perfectly when paralleled without a load division circuit if the regulated voltage of each converter is exactly the same before paralleling. However, this is usually not the case. The real purpose of incorporating a load division circuit in each converter is to assure that load current will be satisfactorily divided for the general case when the regulated voltage of each converter is not exactly the same before paralleling. To assure that the incorporated load division circuit satisfactorily meets this purpose, a series of tests were conducted with the regulated voltage of each converter intentionally set to different levels before paralleling. For one series of tests, one converter no-load output voltage was set at 152 volts d-c and the other converter no-load output voltage was set at 154 volts d-c, prior to paralleling. After paralleling, the converter output voltage became 153 volts d-c which is the average of the two output voltages prior to paralleling. Test results are recorded in Figure 55 for loads from 0 to 125%. The maximum load current

K 1660905

SUBJECT INVERTER / CONVERTER P/N LYP 18293 J 1

CUSTOMER ENGR DEPT. SERIAL NO. B.B. #1

S. O. OR TEST NO. N4-202 D. OR L. SPEC. NO. E2N-5J SHAFT NO. LYP 18293 FRAME NO. B.B. #2

TO DETERMINE OPERATING CHARACTERISTICS OF CONVERTER TRANSDUCTOR

PARA 5.0 SINGLE CONVERTER OPERATION

PARA. 5.5 DC OUTPUT VOLTAGE SET AT 153.5 VOLTS BY ADJUSTING R15 ON EACH UNIT

PARA 5.6 VOLTAGE ACROSS R69 ADJUST TO 20. VOLTS DC. D.C. OUTPUT CURRENT 4.88 AMPS

PARA. 5.7

CONVERTER D.C. OUTPUT CURRENT	B.B. #1	B.B. #2	D.C. VOLTAGE ACROSS R69	BB #1	BB #2
	AMPS	AMPS		VOLTS	VOLTS
	0	0		1.3	1.08
	1.1	1.05		5.3	4.65
	2.0	2.0		8.6	8.4
	3.0	3.0		12.9	12.9
	4.0	4.0		16.8	16.9
	5.0	5.0		20.7	20.7
	6.0	6.0		23.1	23.5

BB #1 R-69 = 1107 Ω BB. # 2 R-69 = 1069 Ω

DC OUTPUT VOLTS - WESTON M341 # 10562 & # 18026 C-R 300

DC OUTPUT AMPS - " M370 # 5982 & # 9257 C-R 5-10

DC VOLTS (R69) - TRIPLETT M630 # 173441 C-R 3-12-60

4 MFD. CAPACITOR ACROSS R69

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Figure 42. Filtered Operating Characteristics of Converter Transductors

K 1660913

SUBJECT INVERTER/CONVERTER P/N LYP 18293 J1 SERIAL NO. B.B. #1

CUSTOMER ENGR DEPT.

S. O. OR TEST NO. N4-202 ~~S. OR I. SPEC.~~ NO. E2N-5J ~~SHAFT NO.~~ LYP18292 ~~FRAME NO.~~ B.B. #2

TO DETERMINE PARALLEL CONVERTER OPERATION PARA. 6.0

PARA. 6.4 + 6.5		EACH UNIT SET AT 153 VOLTS								
PARA 6.4										
#1 DC OUT VOLTS		153	152	152	152	151	141	WESTON	M341	# 10562
#1 DC OUT AMPS		0	1.3	2.57	3.81	5.05	6.28	WESTON	M370	# 5982
#1 DC OUT WATTS	x2	+6	99	197	290	388	444	WESTON	M310	# 14352
#1 DC IN AMPS		3.7	10.9	19.6	28.7	39.6	47.0	(W)	PX5	# 2[illegible]4326
#1 DC IN VOLTS		30.4	29.7	29.1	28.5	27.8	27.5	(W)	PX5	# [illegible]7834
Calculated Current Unbalance			6.5%	4.6%	3%	1.6%				
#2 DC OUT VOLTS		153	152	152	152	151	141	WESTON	M341	# 18026
#2 DC OUT AMPS		0	1.15	2.35	3.6	4.89	6.15	WESTON	M370	# 9257
#2 DC OUT WATTS	x2	-6	87	179	271	366	433	WESTON	M310	# 15925
#2 DC IN AMPS		3.	11.0	19.5	28.0	37.5	47.5	(W)	PX5	# 1975462
#2 DC IN VOLTS		30.1	29.7	29.0	28.6	28.0	27.3	(W)	PX5	# 2000591
LOAD		0	25	50	75	100	125			

PARA. 6.5

OSC. #17 CALIBRATION #1 DC OUT VOLTS AT 153 VOLTS AND #2 DC OUT VOLTS AT 153 VOLTS

#17A CALIBRATION #1 DC OUT AMPS AT 5.0 AMPS AND #2 DC OUT AMPS AT 5.0 AMPS

OSC. #18 PARALLEL UNITS AT NO LOAD PER UNIT

OSC. #19 PARALLEL UNITS AT 25% LOAD " "

OSC. #20 PARALLEL UNITS AT 50% LOAD " "

OSC. #21 PARALLEL UNITS AT 75% LOAD " "

OSC #22 PARALLEL UNITS AT 100% LOAD " "

OSC. #23 PARALLEL UNITS AT 125% LOAD " "

CENTURY OSCILLOGRAPH MODEL 408 Ser. #284

TRACE	Ele Po.	Ele No.	CPS	Calib Res.	Att. Res.	FILM SPEED 33"/SEC.
#1 DC OUT VOLTS	1	W715	2000	46.2Ω	3411Ω	
#1 DC OUT AMPS	5	W213	510	434Ω	7Ω	SEE PAGE K1660904
#2 DC OUT VOLTS	7	A0102	2000	459Ω	3011Ω	FOR TEST SET-UP
#2 DC OUT AMPS	21	W646	510	45.9Ω	28Ω	SCHEMATIC
PARALLEL BRK SIGNAL	17	Y540	1200	18.1	11111Ω	

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Figure 43. Test Results for Parallel Converter Operation

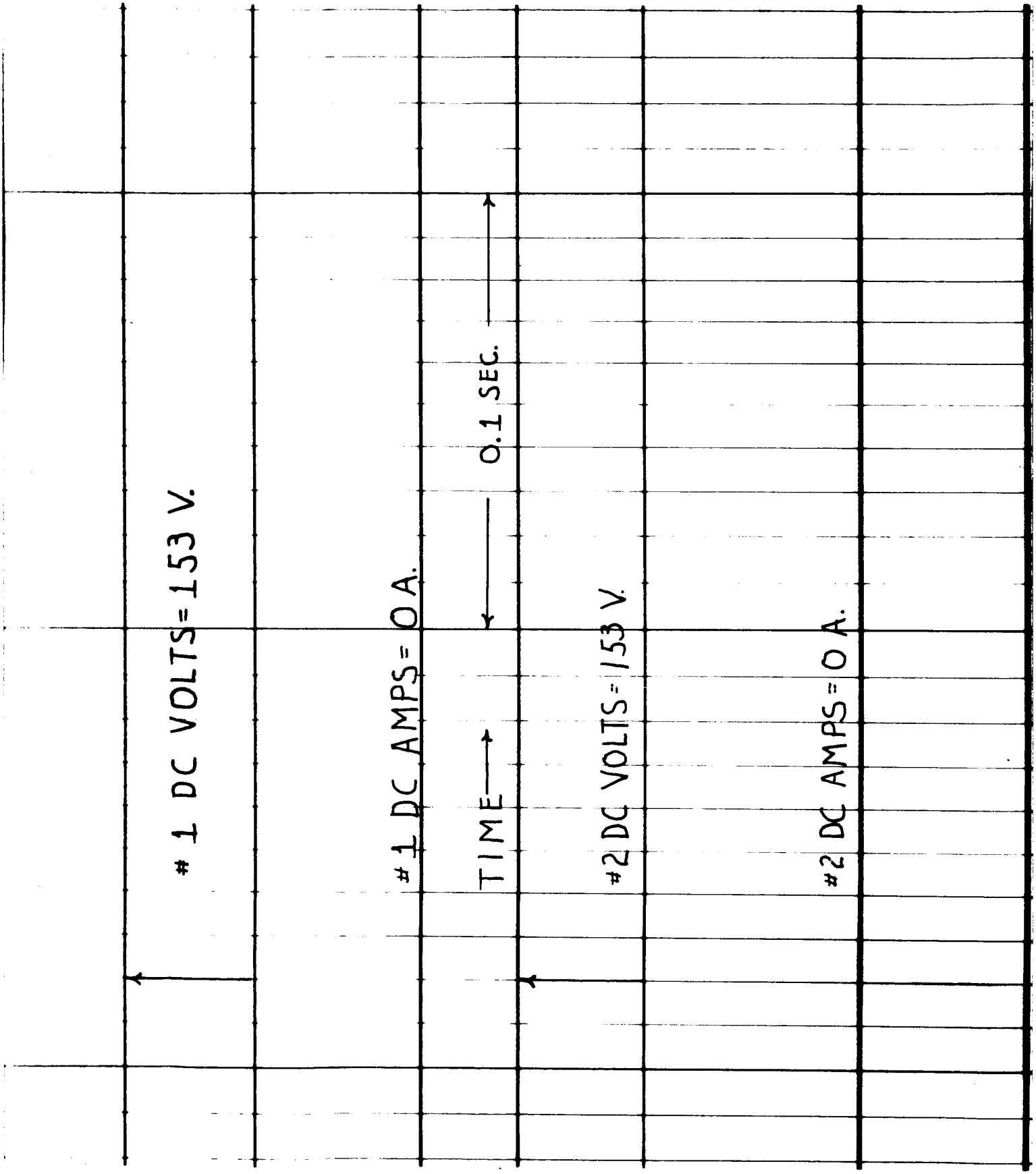

Figure 44. Converter Voltage Calibration Oscillograph Recording (Osc. #17)

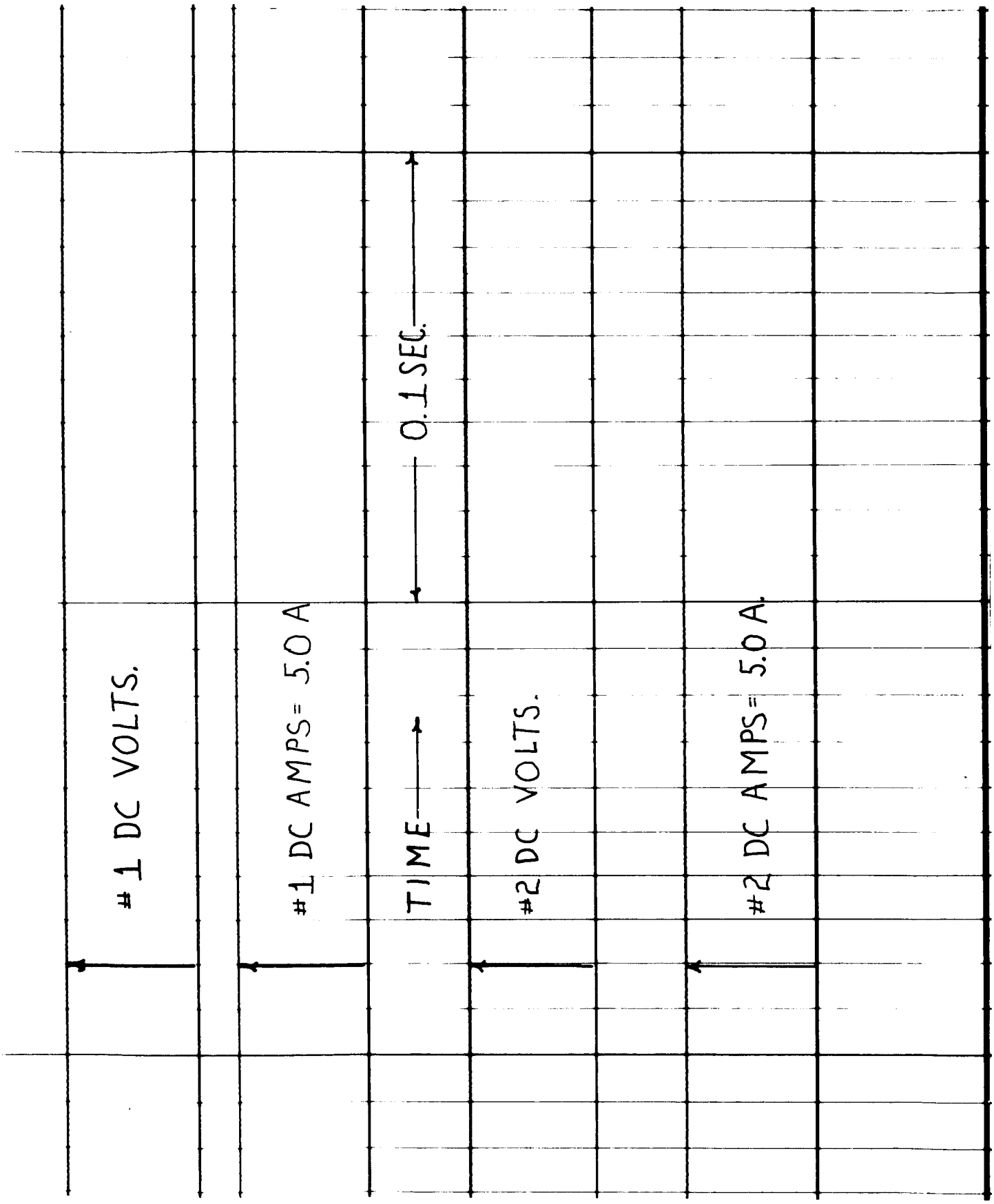

Figure 45. Converter Current Calibration Oscillograph Recording (Osc. #17A)

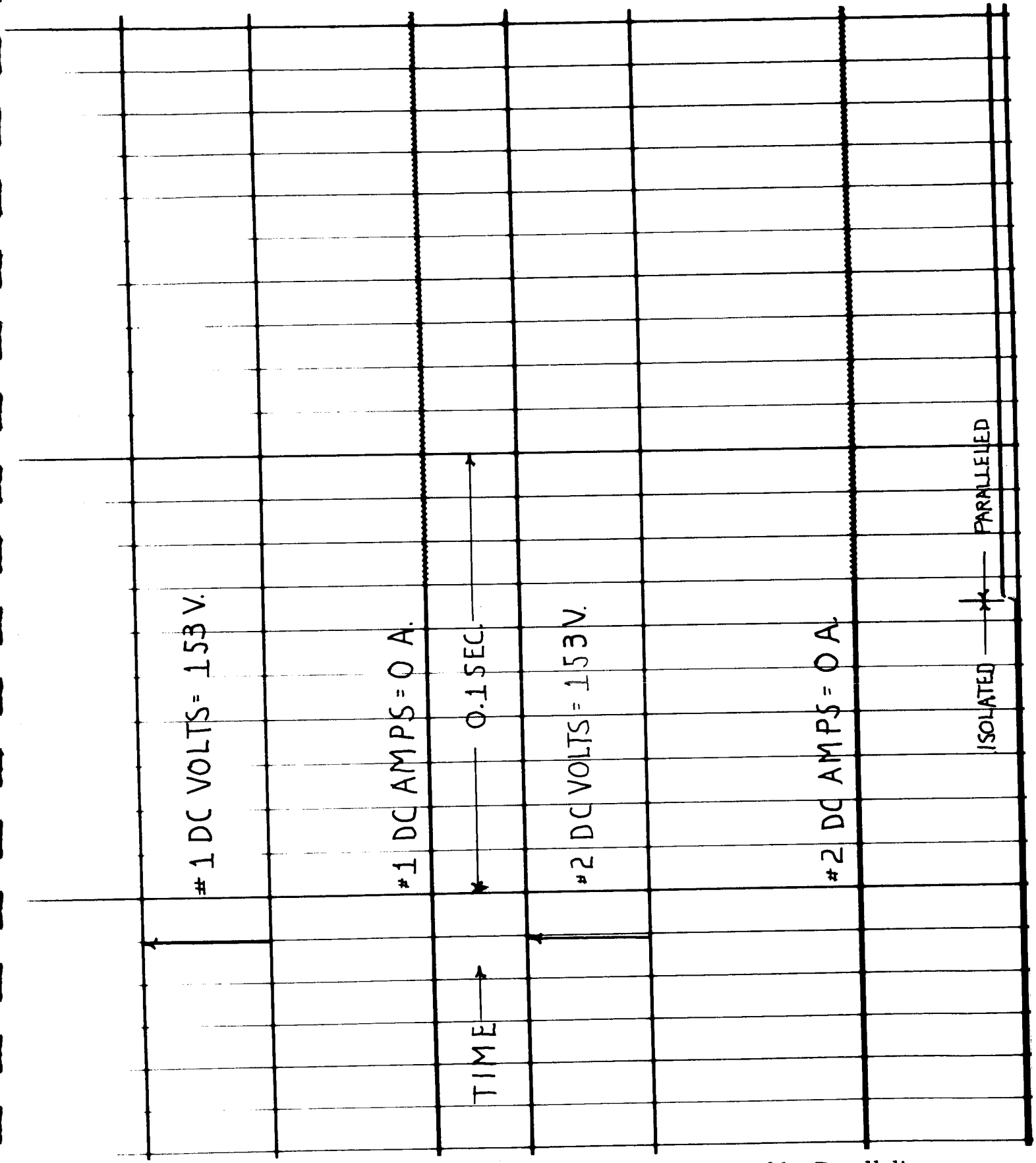

Figure 46. Oscillograph Recording of the Transient Caused by Paralleling Two Static Converters. Each Converter was Unloaded Prior to Paralleling. (Osc. #18)

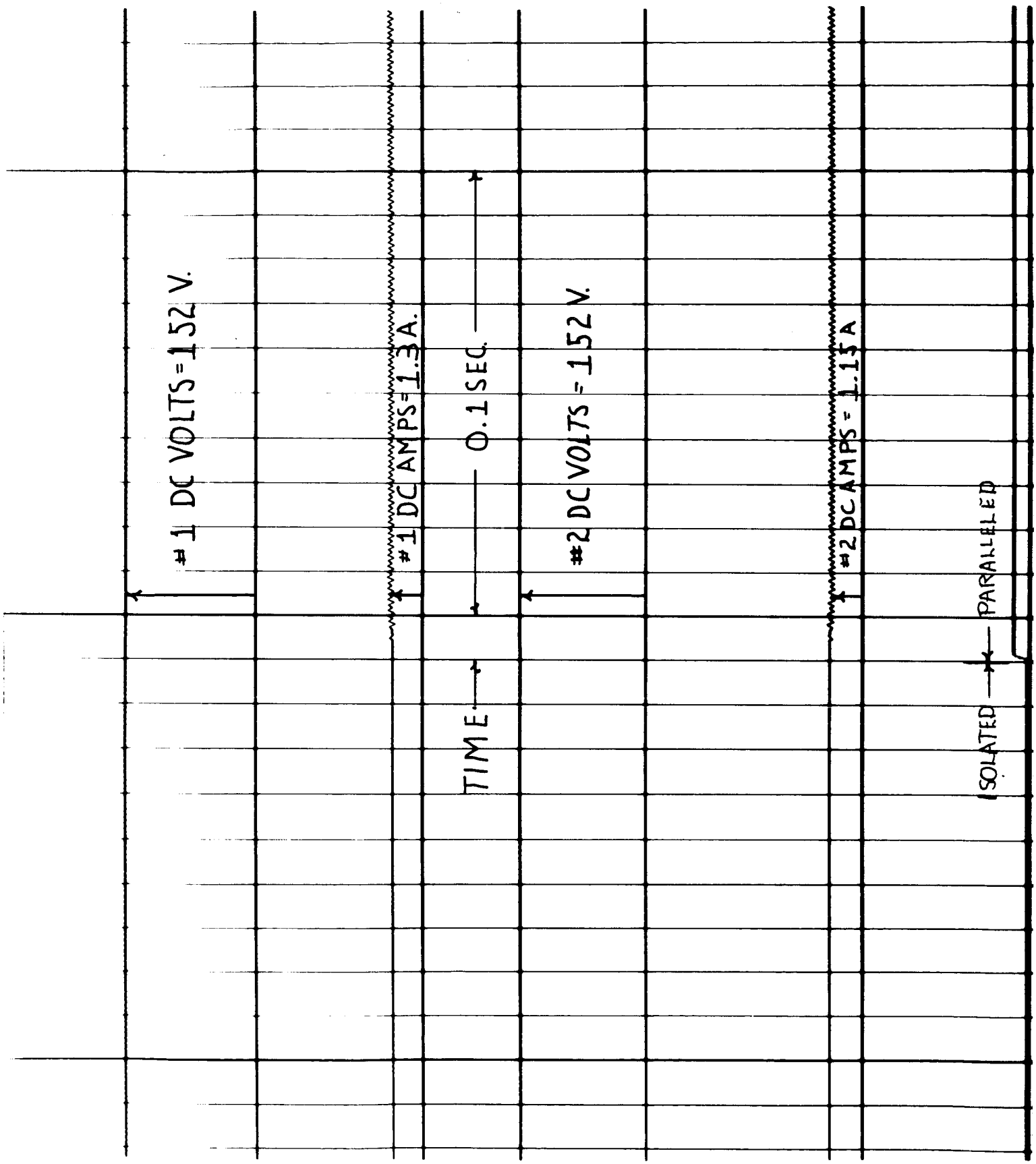

Figure 47. Oscillograph Recording of the Transient Caused by Paralleling Two Static Converters. Each Converter was Loaded with 25% Rated Load Prior to Paralleling (Osc. #19)

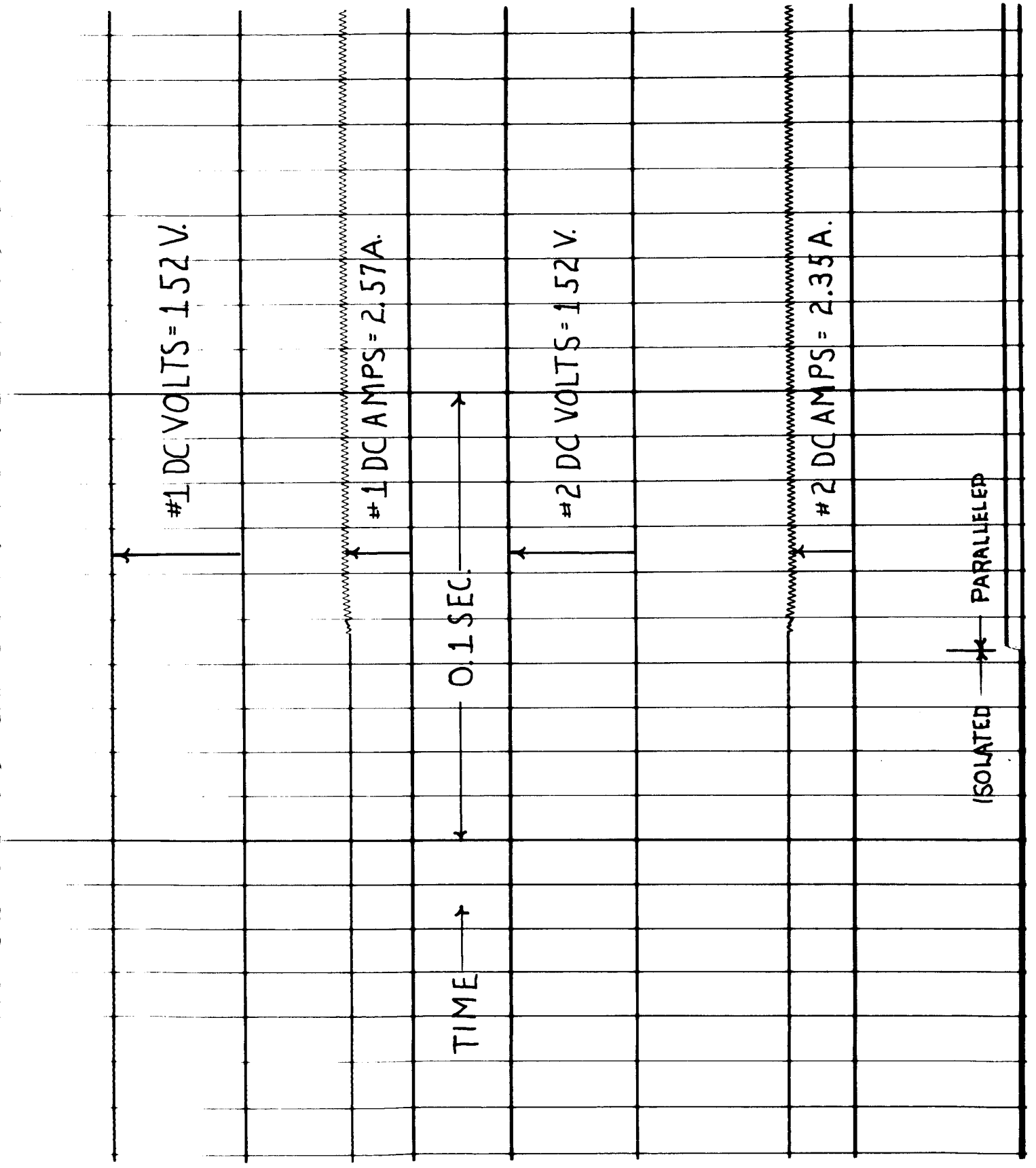

Figure 48. Oscillograph Recording of the Transient Caused by Paralleling Two Static Converters. Each Converter was Loaded with 50% Rated Load Prior to Paralleling (Osc. #20)

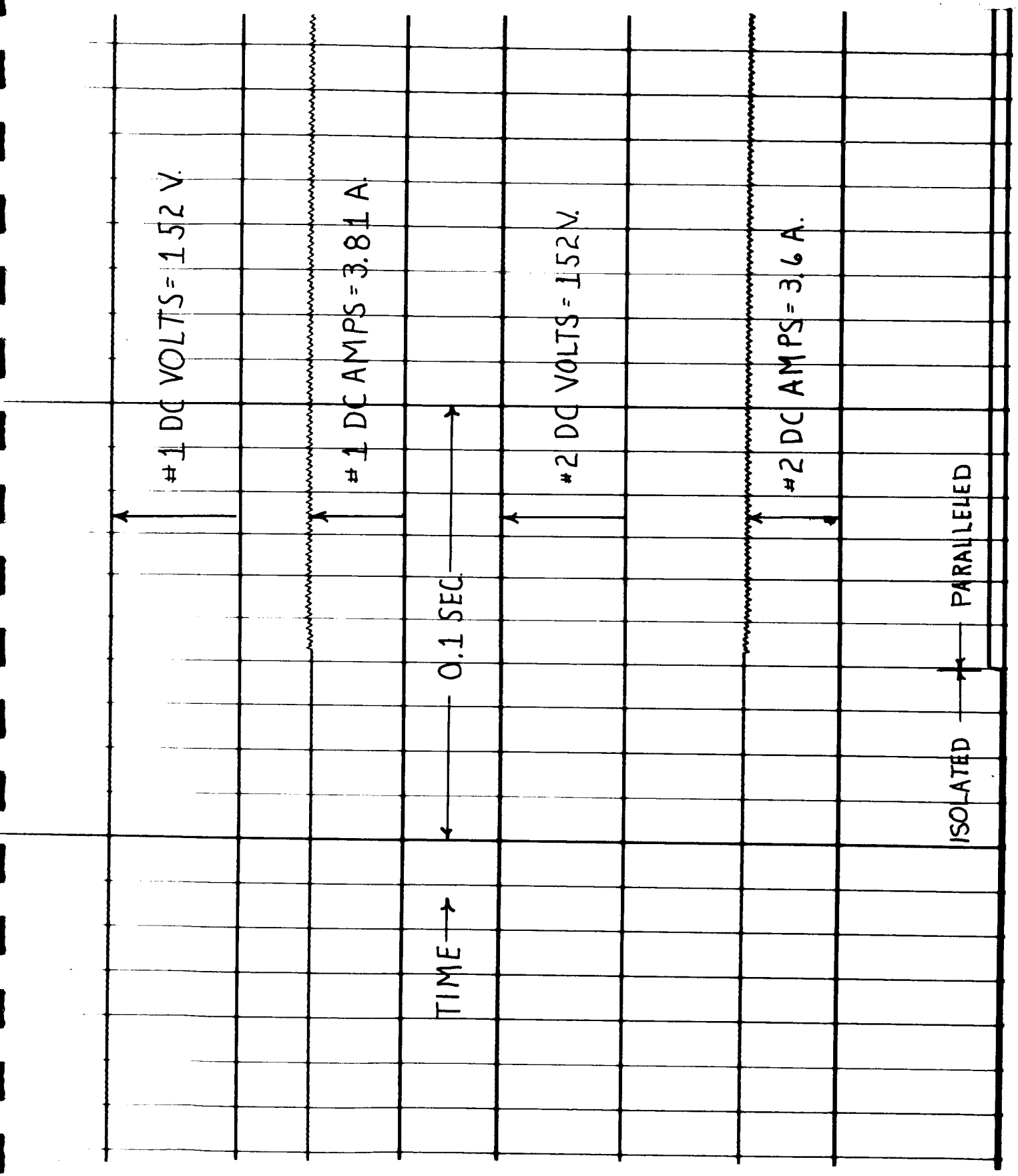

Figure 49. Oscillograph Recording of the Transient Caused by Paralleling Two Static Converters. Each Converter was Loaded with 75% Rated Load Prior to Paralleling (Osc. #21)

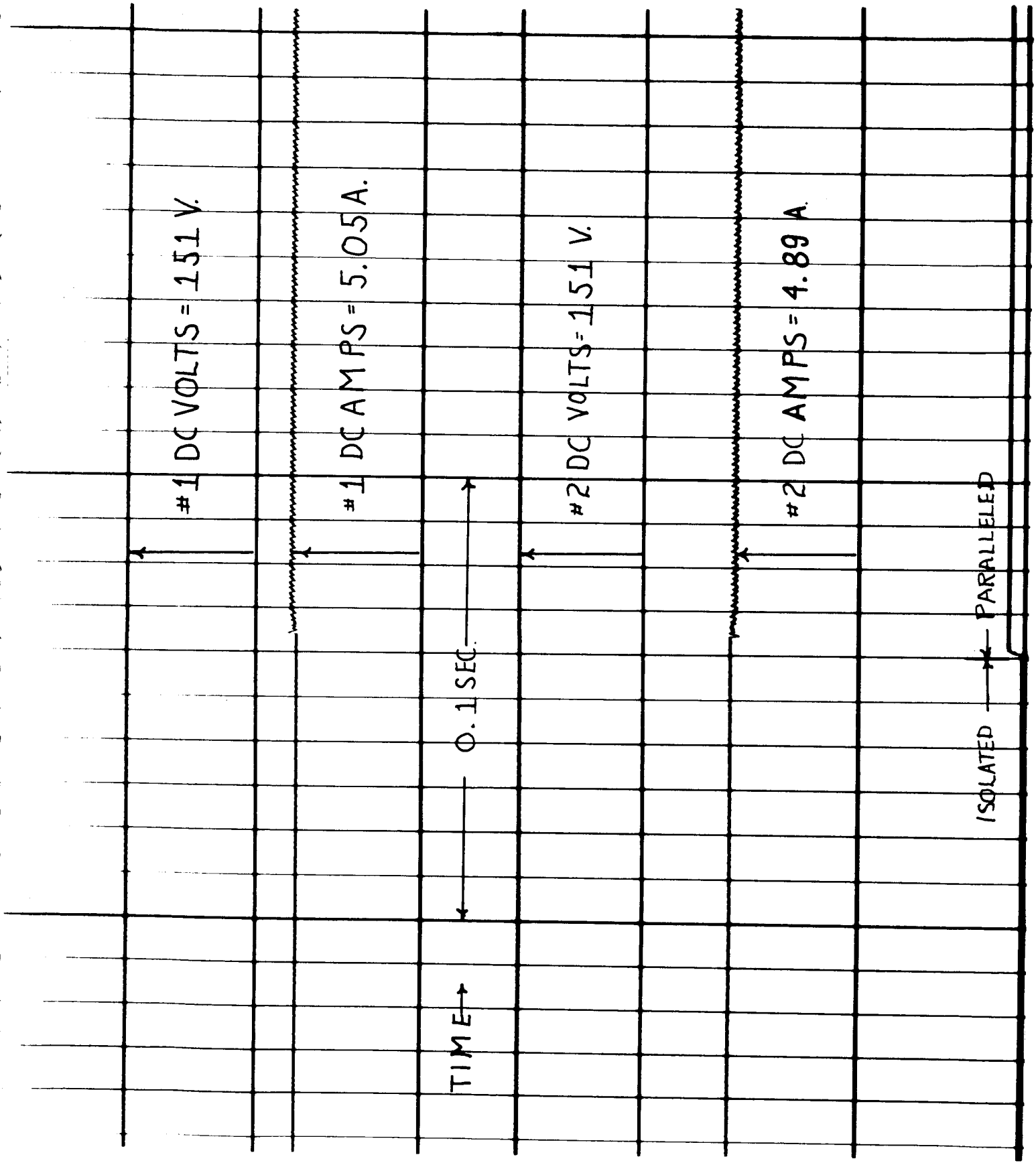

Figure 50. Oscillograph Recording of the Transient Caused by Paralleling Two Static Converters. Each Converter was Loaded with 100% Rated Load Prior to Paralleling (Osc. #22)

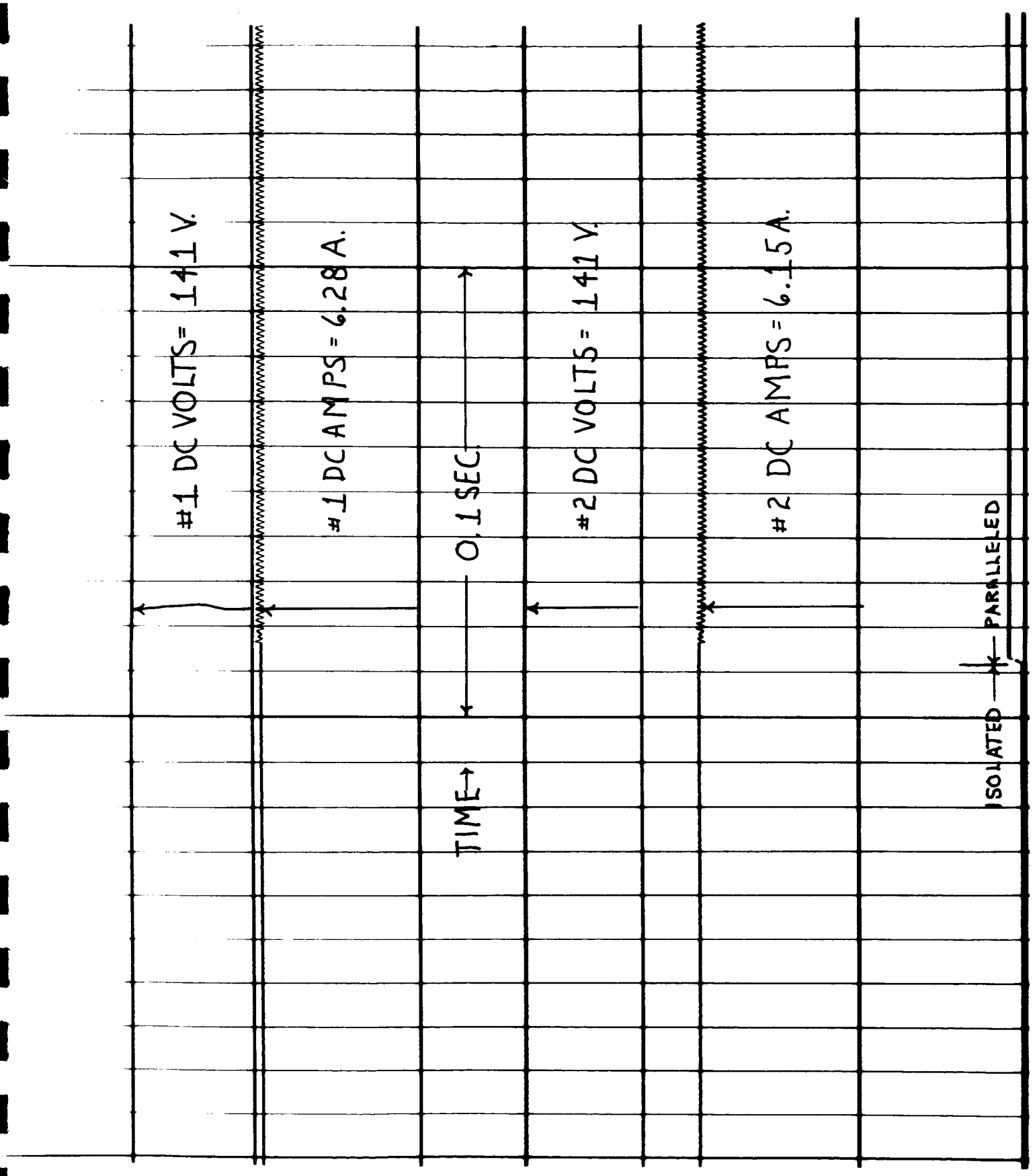

Figure 51. Oscillograph Recording of the Transient Caused by Paralleling Two Static Converters. Each Converter was Loaded with 125% Rated Load Prior to Paralleling (Osc. #23)

K 166091-1

SUBJECT INVERTER/CONVERTER P/N LYPIK2935 1

CUSTOMER ENGR. DEPT. SERIAL NO. B.B. #1

S. O. OR TEST NO. N4-202 D OR I SPEC NO. E2N-5I SHIFT NO. LYPIK292 FRAME NO. B.B. #2

TO DETERMINE PHRALLEL CONVERTER OPERATION PARA 6.0

PARA. 6.6 & 6.7 EACH UNIT SET AT 153 VOLTS

		PARA 6.6		PARA 6.7	
#1 DC OUT VOLTS		152	152	153	151
#1 DC OUT AMPS		4.93	2.58	0	5.05
#1 AC OUT WATTS	X2	375	199	+6	382
#1 DC IN AMPS		38.0	19.8	3.7	39.3
#1 DC IN VOLTS		28.0	29.1	30.4	27.8
#2 DC OUT VOLTS		153	152	153	151
#2 DC OUT AMPS		0	2.41	0	4.95
#2 DC OUT WATTS	X2	0	182	-6	369
#2 DC IN AMPS		3.7	20.5	3.1	39.0
#2 DC IN VOLTS		30.1	29.2	30.2	28.0
LOAD		100			100
		BEFORE PARALLEL	AFTER PARALLEL	OFF	ON
OSC.#		#24		#25	

OSC. #24 #1 CONVERTER LOADED TO 750 WATTS AND #2 CONVERTER AT NO LOAD, PARALLEL UNITS

OSC. #25 #1 & #2 CONVERTERS ARE PARALLELED AT NO LOAD, APPLIED 2 750 WATT LOADS ON & OFF TO THE PARALLELED CONVERTERS.

SEE PAGE K1660904 FOR TEST SET-UP SCHEMATIC
SEE PAGE K1660913 FOR METER DATA, OSCILLOGRAPH DATA AND CALIBRATION FILM.

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Figure 52. Test Results of Paralleling a Loaded Converter with an Unloaded Converter and Placing Rated Load on Two Paralleled-Unloaded Converters

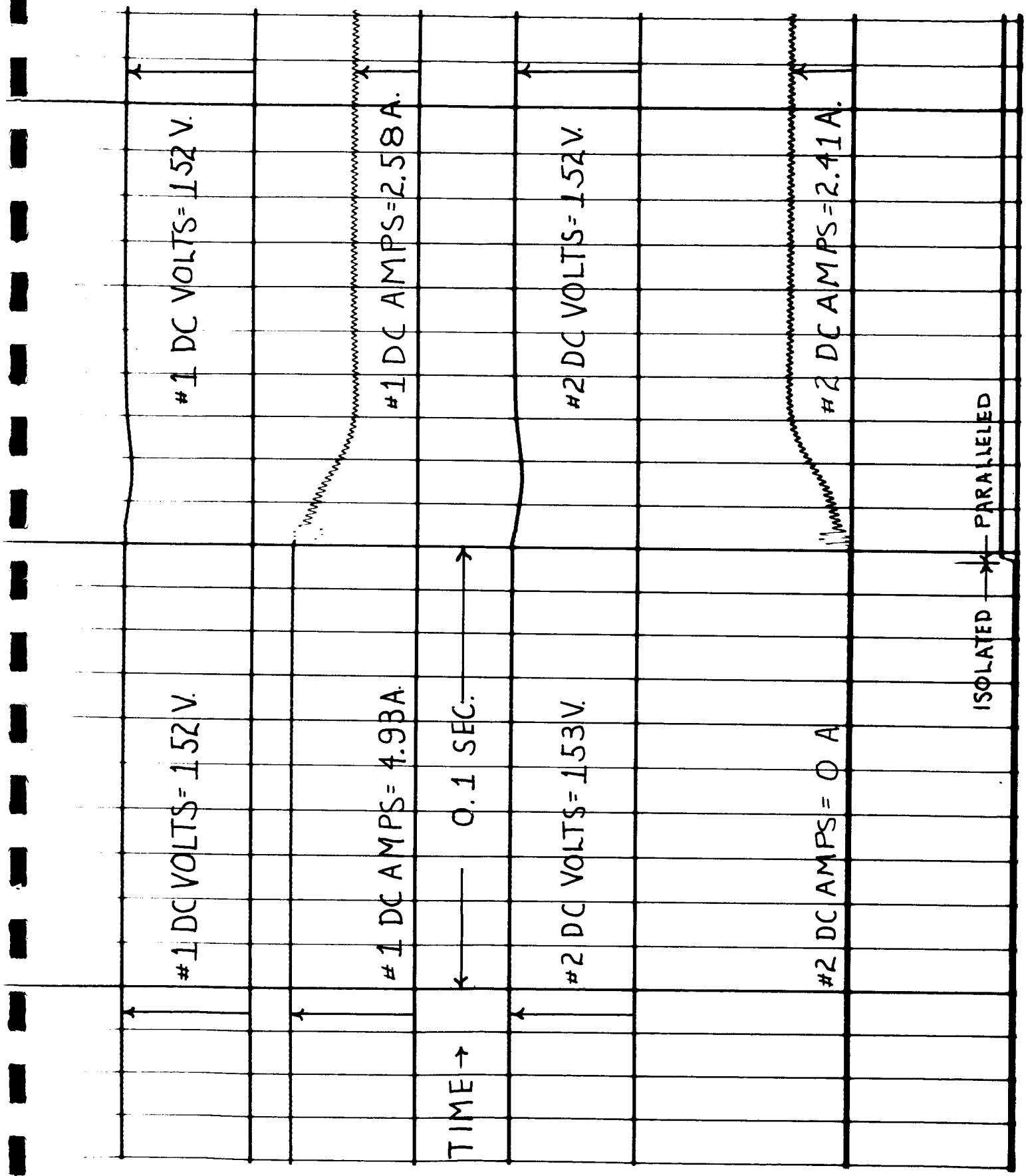

Figure 53. Oscillograph Recording of the Transient Caused by Paralleling a Loaded Converter with an Unloaded Converter (Osc. #24)

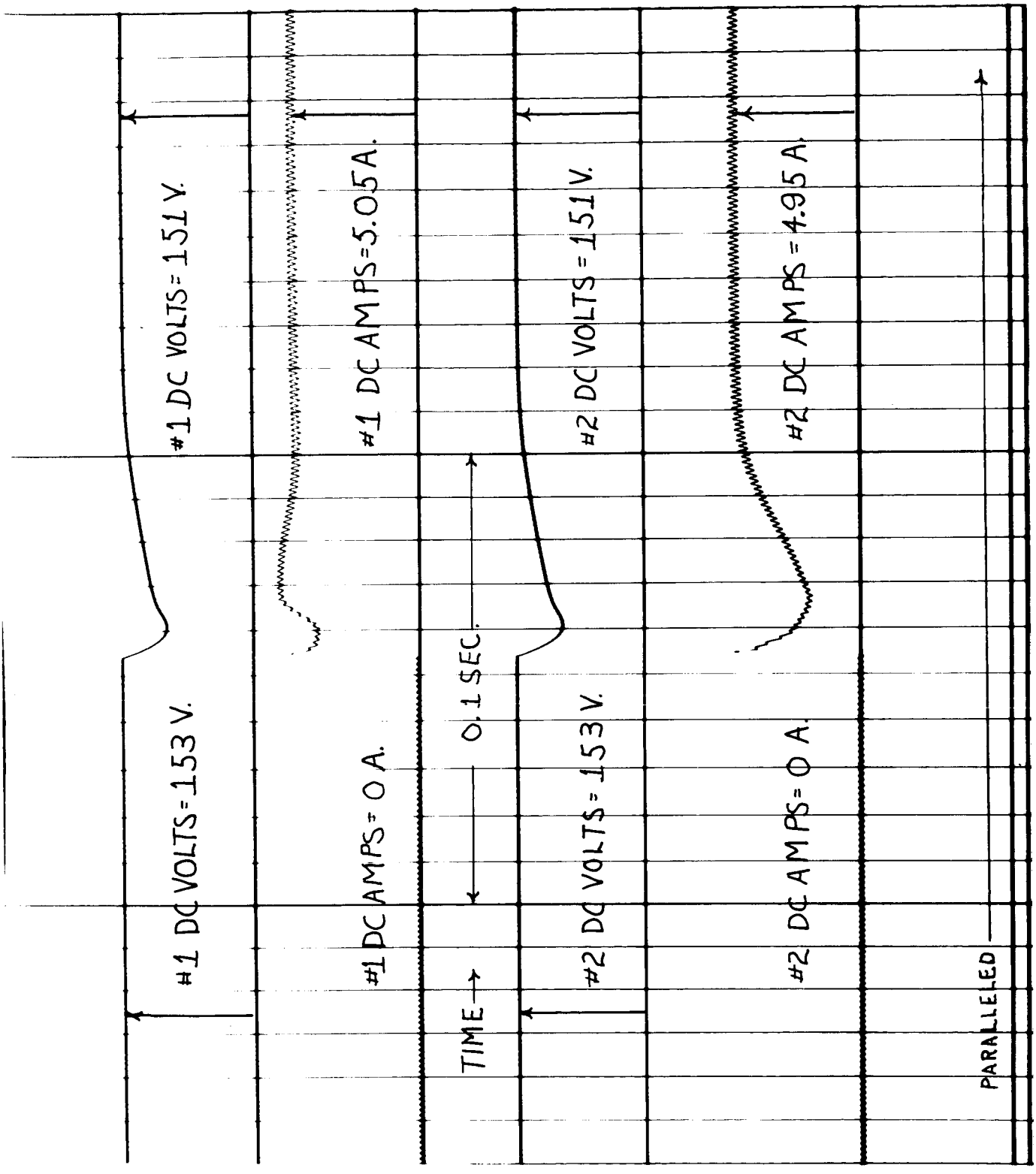

Figure 54. Oscillograph Recording of the Transient Caused by Placing Rated Load on Two Paralleled-Unloaded Converters (Osc. #25)

SUBJECT INVERTER/CONVERTER P/N LYP 18293 J1

CUSTOMER ENGR DEPT SERIAL NO. B.B. #1

S. O. OR TEST NO. N4-202 ~~D. OR L. SPEC. NO.~~ E2N-5J SHAFT NO. LYP/18292 FRAME NO. B.B. #2

TO DETERMINE PARALLEL CONVERTER OPERATION PARA. 6.0

PARA 6.4	#1 SET AT	152 V		#2 SET AT	154 V		
#1 DC OUT VOLTS	153	152	152	151.5	151	140	
#1 DC OUT AMPS	0	1.25	2.5	3.77	5.0	6.25	
#1 DC OUT WATTS X2	0	95	193	290	380	490	
#1 DC IN AMPS	2.7	10.5	19.1	28.6	38.6	47.5	
#1 DC IN VOLTS	30.4	29.6	29.1	28.4	27.8	27.3	
Calculated Current Unbalance		2%	2%	1.2%	1.0%		
#2 DC OUT VOLTS	153	152	152	151.5	151	140	
#2 DC OUT AMPS	0	1.2	2.4	3.68	4.9	6.15	
#2 DC OUT WATTS X2	0	92	183	279	367	489	
#2 DC IN AMPS	3.6	11.5	20.	29.	39.	47.5	
#2 DC IN VOLTS	30.1	29.7	29.1	28.5	28.	27.4	
LOAD	0	25	50	75	100	125	

OSC. #26 #1 & #2 CONVERTERS WITH 100% LOAD ON EACH AND PARALLEL UNITS

SEE PAGE K1660904 FOR TEST SET-UP SCHEMATIC

SEE PAGE K1660913 FOR METER DATA, OSCILLOGRAPH DATA AND CALIBRATION FILM.

PREVIOUS TEST PAGE

3-16-64 R. Marks-A. Stevenson G. ERMBELSTR

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Figure 55. Test Results for Parallel Converter Operation with No-Load Converter Output Voltages Preset at 152 and 154 Volts D-C Prior to Paralleling

unbalance was 2%. Figure 56 is an oscillograph recording of the paralleling transient with 100% load connected to each converter prior to paralleling.

For a final series of tests one converter no-load output voltage was set at 148 volts d-c and the other converter no-load output voltage was set at 158 volts d-c prior to paralleling. After paralleling, the converter output voltage became 154 volts d-c which is nearly the average of the two output voltages prior to paralleling. The results for this series of tests are recorded in Figures 57 and 58. The maximum load current unbalance was 17.3% which is very good for these test conditions.

NOTE: The signal which appears on the bottom of all converter paralleling oscillographs to indicate whether the converters are paralleled or isolated is controlled by an auxiliary contact on the paralleling breaker. This signal occurs from 3 to 5 milliseconds before the converters appear to be paralleled (see Figures 46 through 51 for examples). It is believed that the particular breaker used for paralleling the converters had this characteristic. That is, the auxiliary contacts actually closed before the main contacts closed. This was not noticeable with the breaker used to parallel the inverters.

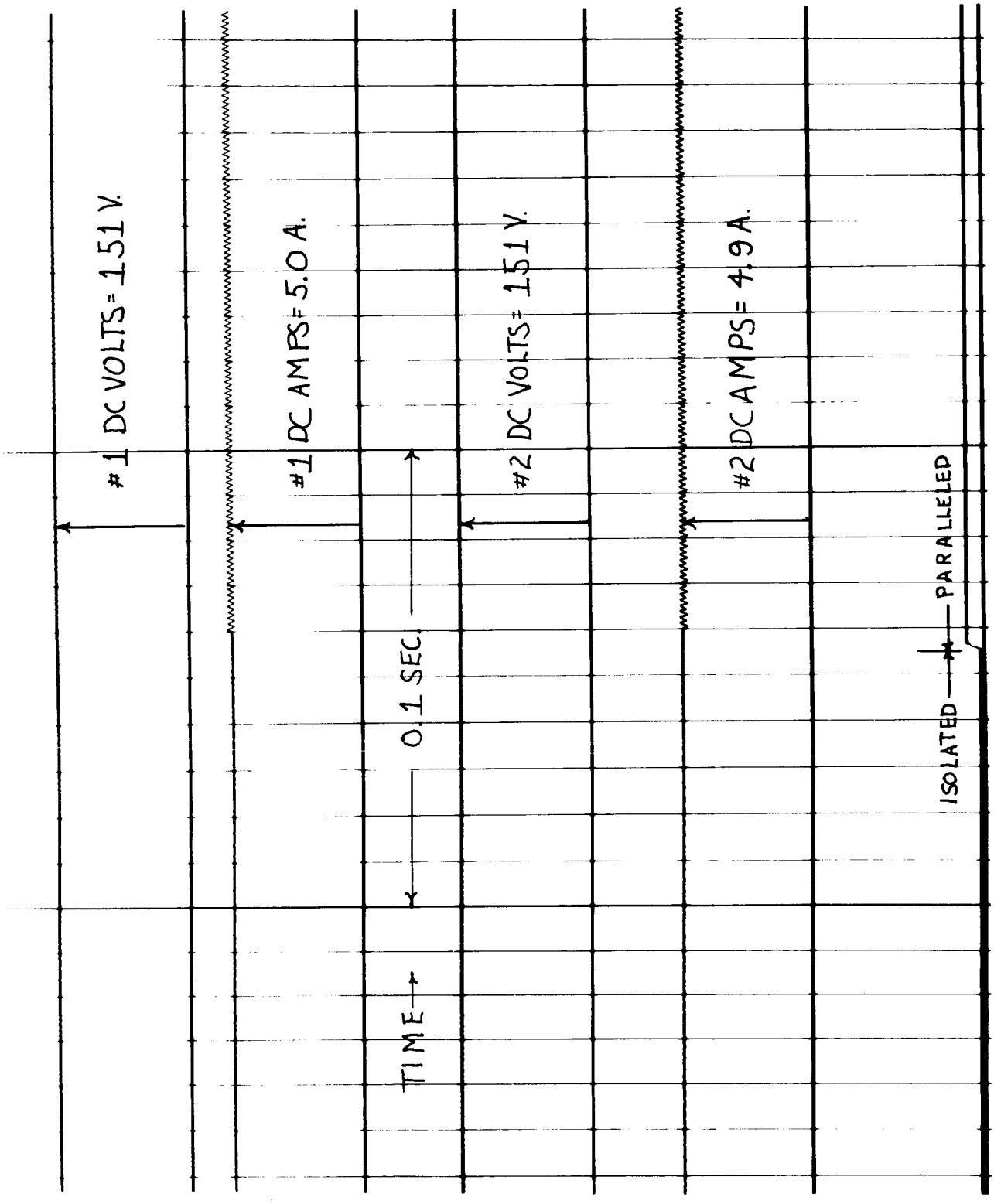

Figure 56. Oscillograph Recording of the Paralleling of Two Fully Loaded Converters Whose No-Load Output Voltages Had Been Preset at 152 and 154 Volts D-C Prior to Paralleling (Osc. #26)

K 1660911

SUBJECT INVERTER/CONVERTER P/N LYP18293J1

CUSTOMER ENGR. DEPT. SERIAL NO. B.B. #1

S. O. OR TEST NO. N4-202 SPEC. NO. E2N-5J ~~DRAFT NO.~~ LYP18292 FRAME NO. B.B. #2

TO DETERMINE PARALLEL CONVERTER OPERATION PARA. 6.0

PARA 6.4	#1 SET AT	148V	#2 SET AT	158V			
#1 DC OUT VOLTS		154	152	151	151	150	138
#1 DC OUT AMPS		0	1.0	2.3	3.54	4.82	6.2
#1 DC OUT WATTS	X2	+5	77	176	270	365	435
#1 DC IN AMPS		2.8	9.0	17.5	26.6	37.0	46.5
#1 DC IN VOLTS		30.4	29.7	29.1	28.6	27.9	27.3
Calculated Current Unbalance			17.3%	6.1%	4.0%	2.8%	
#2 DC OUT VOLTS		154	152	151	151	150	138
#2 DC OUT AMPS		0	1.43	2.61	3.84	5.1	6.25
#2 DC OUT WATTS	X2	-5	109	199	290	385	438
#2 DC IN AMPS		4.5	13	21.6	30.	41.0	48.5
#2 DC IN VOLTS		30.	29.4	28.8	28.3	28.8	27.3
LOAD		0	25	50	75	100	125

OSC. #27 1 & 2 CONVERTER WITH 100% LOAD ON EACH AND PARALLEL UNITS

SEE PAGE K 1660904 FOR TEST SET-UP SCHEMATIC

SEE PAGE K 1660913 FOR METER DATA, OSCILLOGRAPH DATA AND CALIBRATION FILM.

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Figure 57. Test Results for Parallel Converter Operation with No-Load Converter Output Voltages Preset at 148 and 158 Volts D-C Prior to Paralleling

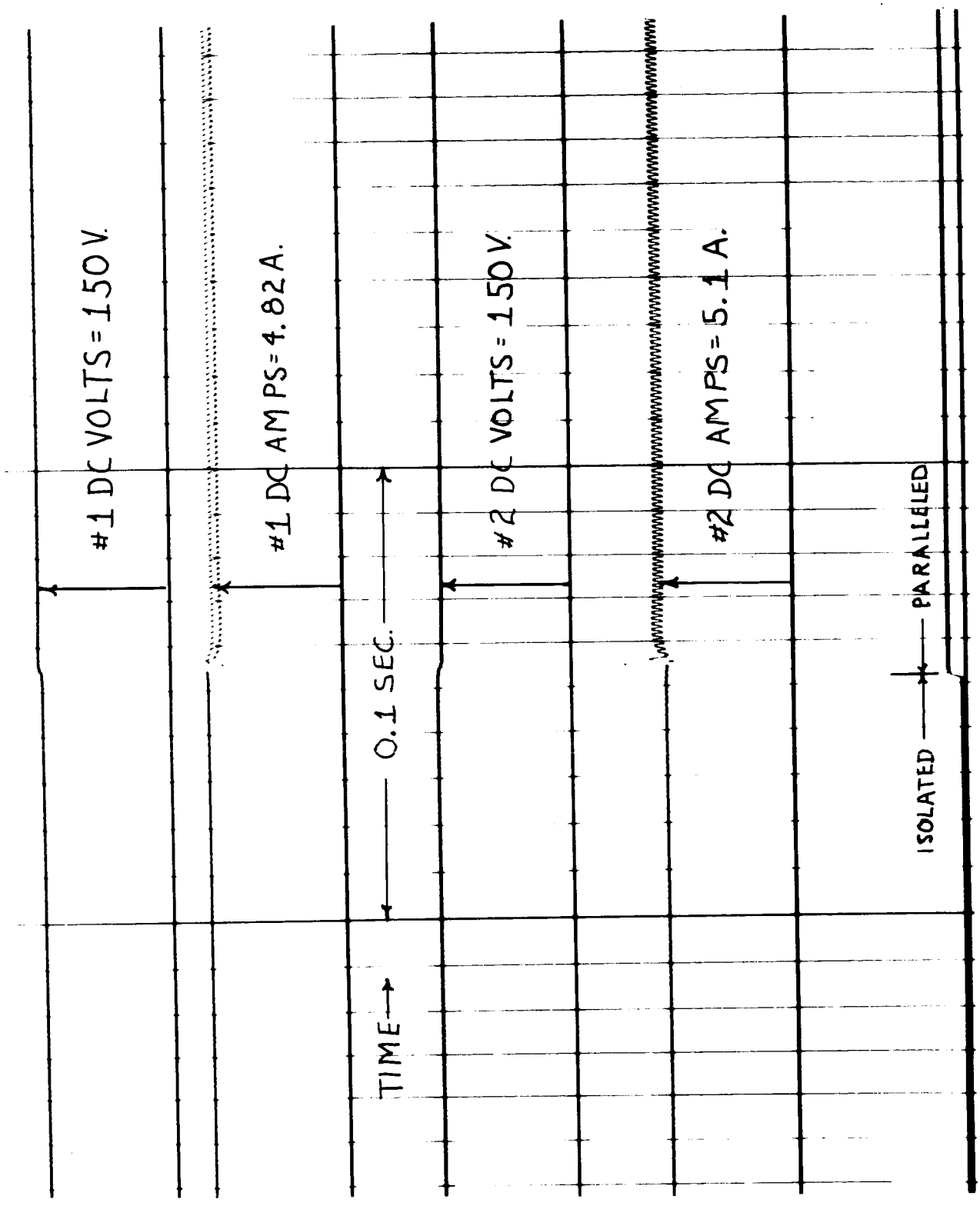


Figure 58. Oscillograph Recording of the Paralleling of Two Fully Loaded Converters Whose No-Load Output Voltages Had Been Preset at 148 and 158 Volts D-C Prior to Paralleling (Osc. #27)

IV. WEIGHT REDUCTION AND RELIABILITY IMPROVEMENT BY PARALLELING STATIC INVERTERS

This part of the report presents an analysis of the factors involved in achieving higher reliability and reduced weight in moderate power static-inverter systems. Several system configurations are discussed, and numerical examples are given to highlight the advantages and disadvantages of each arrangement. The intention is to provide general background information that will help the system designer decide the direction of future study efforts and specify the best system configuration for a particular application. The discussion is concerned specifically with d-c to a-c static-inverter systems operating at power levels suitable for spacecraft auxiliary power, although many of the principles discussed are applicable to other kinds of inverter systems; for example, d-c to d-c conversion in the megawatt range, as required for spacecraft electric propulsion.

Three types of systems are considered in the following discussion. They are:

1. Single inverter, handling full system power.
2. Several inverters; one operating and the rest used as standby, or backup, units.
3. Several inverters operating in parallel.

The choice of the best system depends on many factors. For this reason, the three kinds of systems will be discussed separately and the factors affecting weight and reliability of each will be described. Comparisons between the different systems will then be made to point out the primary advantages and disadvantages of each configuration.

A. Factors Affecting Weight and Reliability of a Single Static-Inverter.

The most important factor affecting the weight of an inverter is its power rating. In general, higher power capacity is achieved through using larger and heavier electrical parts. These parts, in turn, require more massive mechanical supporting members.

Another factor is the quality of power required from the inverter. Accurate voltage and frequency regulation, phase displacement regulation and low harmonic content all require additional electrical components, which add weight. Some inverters, designed for the relatively undemanding task of driving induction motors, allow a drastic weight reduction by eliminating all power transformers and filters. This is an extreme example of the effect of power quality on weight.

The means of cooling and the temperature of the cooling medium will affect the weight of an inverter. As the temperature of the coolant approaches the operating temperature of the inverter components, the inverter weight rises sharply. However, for reasonably low coolant temperatures, the particular cooling system used will not have a very large effect on inverter weight. The appropriate kind of cooling system is usually determined on bases other than minimizing inverter weight.

Another variable is input voltage. There is an optimum input voltage for every inverter design, and wide variance from the optimum causes reduced efficiency and increased weight. A desirable input voltage for transistor inverters is 56 volts.

Unlike an electrodynamic inverter (motor-generator), a static inverter has very little inherent capacity for overload. If the inverter is required to carry overloads, the weight goes up considerably, because the unit must be designed essentially for the peak power requirement, rather than the normal load.

There are many other things that affect the weight of a single inverter, but the above considerations are the major ones.

With so many factors modifying the basic weight to power relationship, it is not possible to predict the weight of a new inverter design with any great accuracy, without actually going through the complete design process. However, to meet the need for some standard of reference to be used in the numerical examples given later in this report, a curve has been prepared showing typical values of weight vs. power rating for static inverters. This curve, Figure 59, has been drawn on the basis of empirical data and represents, approximately, the present state-of-the-art. The equation of the curve, $Wgt = 33(KVA)^{0.59}$, results from inspection of the graph, and not from any theoretical consideration.

Several of the factors that affect weight also affect reliability. In particular, any electrical parts that are added to accomodate varying input voltages or to provide higher quality output power will reduce reliability. The means of cooling, and more especially the operating temperature, will have an important effect on reliability. Higher operating temperatures reduce inverter reliability, because the reliability of all electrical components is reduced by elevated temperatures.

Environmental conditions, such as vibration, temperature cycling and acoustic noise will affect the inverter's reliability by causing material fatigue and thermal stresses.

Electrical design has a strong influence on reliability. Proper choice of components, simplicity, use of protective devices, use of redundancy and worst case design are some of the techniques used to increase the reliability of an inverter.

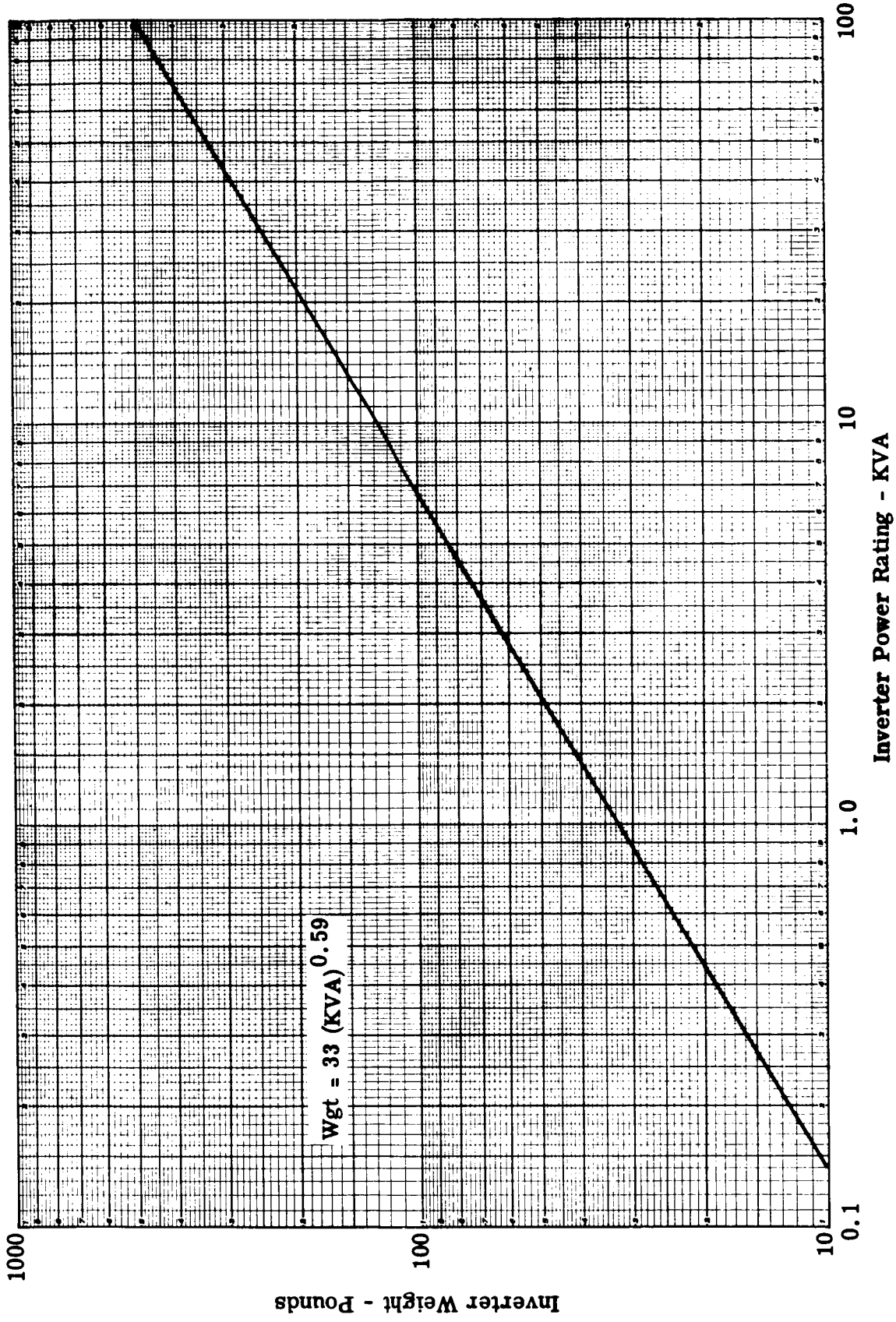


Figure 59. Typical Weight Vs. Power Rating of Static Inverters

In the final analysis however, the determining factor in reliability is time. The Department of Defense defines reliability as, "The probability that a piece of equipment will give satisfactory performance for a specified period of time, under specified operating conditions". This is the definition to be used in this report. The lifetime of a piece of equipment, such as an inverter, is usually thought to be composed of three periods. The first period is the early failure, or "burn-in" portion. The second is the so called "random-failure" period, and the third is the end-of-life or "wearout" period. The failure rate is high during the first and third periods and relatively low during the second period. Usually an inverter to be used in as critical an application as spacecraft auxiliary power would be tested for a considerable time prior to launch; long enough to cover the early-failure portion of its life. Also, the duration of the mission would be expected to be short enough so that the wearout period would not be reached. Thus, attention is concentrated on the random-failure portion of the inverter's lifetime.

During this period, the reliability of the inverter may be described as a function of time. The equation is

$$(28) \quad R = e^{-ft} = e^{-\frac{t}{MTBF}}$$

where R is reliability

t is time

f is failure rate

MTBF is mean time between failures, or mean time to failure of a non-repairable item.

The applicability of this equation to complex electrical equipment has been theoretically and empirically demonstrated and is generally accepted. The equation is plotted in Figure 60 to show graphically the dependence of reliability upon time. The units of time on the horizontal axis are MTBF units. The ordinate, reliability, is the probability that the inverter survives for the specified period of time, assuming it was operating successfully at time zero. An interesting feature of this curve is that time zero may be defined at any point during the random-failure portion of the inverter operating life. That is, the probability that the inverter will survive for a specified period of time does not depend on how long the unit has been operating previously. The only criterion is that it be operating at the moment the observation is begun.

The reliability curve and the weight curve will be used in numerical examples, after the multiple-inverter power systems are discussed.

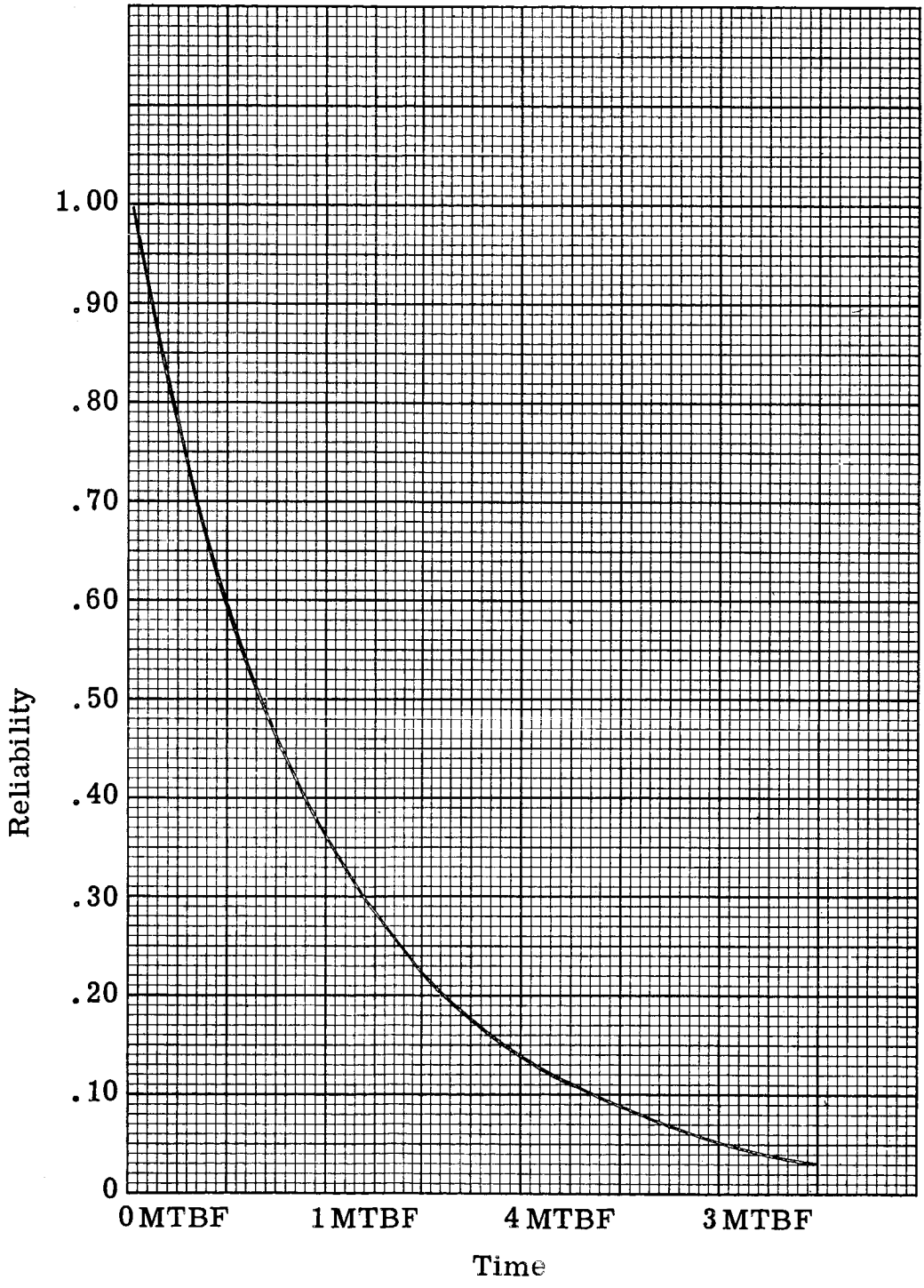


Figure 60. Reliability Vs. Time for the Exponential Distribution

B. Factors Affecting Weight and Reliability of Multiple Inverter Systems Using Standby Redundancy.

Inverter systems using standby redundancy may be described as follows. Several inverters are carried aboard the spacecraft. Each of these units is capable of handling the full power load. The first unit operates until it fails, when an automatic changeover circuit will place the second unit in operation. If the second inverter fails, the third unit is started, etc. Thus, if the system contains N inverters, N-1 changeover circuits are required.

This kind of system utilizes the simplest form of redundancy, and is capable of much higher reliability than a system having only one inverter. In theory, any desired degree of reliability may be obtained, simply by incorporating a sufficient number of properly designed inverters. To achieve the best reliability, the changeover circuits must also have high reliability. Any unreliability in the changeover circuits will reduce the reliability of the system. However, it should be feasible to make a changeover circuit having a relatively small failure rate, because the number of parts can be much smaller than the number of parts used in an inverter. In a manned vehicle, the changeover function would probably be performed by a man. However, this report assumes an electronic changeover device.

The reliability and weight of the standby type of system depend upon the weight and reliability of the individual inverters and changeover circuits, and upon the total number of units used. Obviously, it is desirable to begin with the most reliable inverter design that is available. Considering only the straightforward types of inverter designs, i.e., those having no internal redundancy, the most reliable design should not necessarily weigh any more than the less reliable ones. The actual weight of the inverter will depend on the several factors mentioned earlier, chief among them being power rating.

Given an inverter of sufficient power rating, equal to the system power rating, and a reasonably high reliability, the next requirement is a changeover circuit having high reliability and light weight. This should present no particularly difficult technical problems because, as mentioned earlier, the changeover circuit may be made with relatively few parts, operating at a low stress level.

Once the basic building blocks are available, it is a straightforward matter to determine the system configuration. The reliability of the system depends upon the reliability of the component parts, according to the following equation, derived in Appendix III.

$$R_S = 1 - (1 - R_I)(1 - R_I R_C)^{n-1} \quad (29)$$

where R_S = system reliability

R_I = inverter reliability

R_C = changeover circuit reliability

n = number of inverters in system

$n-1$ = number of changeover circuits in the system

The various reliabilities are calculated from equation (28) assuming the failure rates are constant.

The use of the above equations will be illustrated by a numerical example. This example has further application to the present discussion.

Example #1.

A. Suppose that a system is contemplated whose power requirement is such that a single inverter can carry the full power load.

B. Further, suppose that a reliability calculation has shown that the inverter has an MTBF of 5,000 hours, under the expected conditions of operation.

C. Suppose that a changeover circuit has been designed, having a calculated MTBF of 60,000 hours, under the expected operating conditions.

Question:

If the mission duration is 1,000 hours, and the required reliability of the inverter system is 0.99, how many inverters must be used in a standby configuration?

Solution:

Solve equation (29) for n.

$$n = 1 + \frac{\left(\log_e \frac{1-R_S}{1-R_I}\right)}{\left(\log_e 1-R_I R_C\right)}$$

R_S (specified) = 0.99

From equation (28):

$$R_I = e^{\frac{-1000}{5000}} = 0.8185$$

$$R_C = e^{\frac{-1000}{60,000}} = 0.9835$$

$$\log_e \frac{1-R_S}{1-R_I} = \log_e \frac{0.01}{0.1815} = -2.90$$

$$\log_e (1-R_I R_C) = \log_e (0.195) = -1.635$$

$$n = 1 + \left(\frac{-2.90}{-1.635}\right) = 1 + 1.77$$

$$n = 2.77$$

The results state that 2.77 inverters must be used. Obviously, the choice amounts to using 2 inverters and accepting poorer reliability than specified, or using 3 and accepting a weight penalty.

It is precisely this kind of situation that is alleviated by having the ability to parallel inverters. The numerical example will be extended in the next section, to demonstrate the advantage of a parallel inverter configuration.

C. Factors Affecting Weight and Reliability of Paralleled Inverters.

The first requirement is a means for successfully operating the inverters in parallel. In addition there must be an automatic protection circuit that will assure that a failed inverter will be removed from service before it can cause trouble in the rest of the system. The first of these requirements has been accomplished and is the concern of the main part of the present study contract. The task of developing the means for automatic paralleling and protection has been added to this contract and will be the subject of the next quarterly report. For the present, it is assumed that both the means for paralleling and the means for automatic protection are at hand.

The numerical example that follows will demonstrate one of the advantages of paralleled inverters: specifically that the system may be tailored closely to the reliability specification, eliminating the dilemma encountered in the preceding example. Further advantages of parallel systems will be discussed after completion of the example.

Example #2.

Suspose a system is to be designed to perform the same function as the system of Example #1, except that four inverters are to be used, operating in parallel.

A. Inverter MTBF remains at 5000 hours.

B. Mission duration remains at 1000 hours.

C. Required reliability remains 0.99.

Assume that an automatic paralleling and protection scheme has been designed, having an MTBF of 25,000 hours (comparison to 60,000 hours for standby changeover scheme reflects greater complexity expected in paralleling scheme).

Question:

If two of the four inverters may fail without causing system failure, what will be the system reliability and weight? Compare to the previous example.

To solve this problem, an additional equation is required; the binominal expansion.

Let R = reliability (of an item)

Q = unreliability (probability of failure)

By definition $R+Q = 1$

Hence $(R+Q)^n = 1^n = 1$

For a system containing four items,

$$(R+Q)^4 = 1$$

Expanding:

$$(30) \quad R^4 + 4QR^3 + 6Q^2R^2 + 4Q^3R + Q^4 = 1$$

The terms of the equation express the following relationships:

R^4 = probability of exactly 0 failures out of 4 items.

$4QR^3$ = probability of exactly 1 failure out of 4 items.

$6Q^2R^2$ = probability of exactly 2 failures out of 4 items.

$4Q^3R$ = probability of exactly 3 failures out of 4 items.

Q^4 = probability of exactly 4 failures of of 4 items.

The proof of this interpretation is too lengthy to be presented here and can be found in Statistical Quality Control by E. L. Grant (2nd Ed., McGraw Hill, 1952, pg 204) and several other texts and reports.

In the particular example under discussion, the system will fail only under two conditions: (A) if 3 out of 4 items fail, or (B) if 4 out of 4 items fail. Hence, the probability of system failure $Q_{SP} = 4Q^3R + Q^4$ and the system reliability $R_{SP} = 1 - Q_{SP}$. It remains to find the values of Q and R.

Let an "item" be defined as an inverter and its associated set of paralleling and protection circuits.

$R_I = 0.8185$, from the previous example

R_P = reliability of paralleling circuit

$$R_P = e^{-\frac{t}{MTBF}} = e^{-\frac{1}{25}} = 0.9608$$

Then $R = R_I \cdot R_P = 0.786$

$$Q = 1 - R = 0.214$$

$$Q_{SP} = 4Q^3R + Q^4 = 0.00518$$

$$R_{SP} = 1 - Q_S = 0.99482 = \text{system reliability}$$

This is adequate to meet the specification.

To make a comparison of weights, Figure 59 will be used together with some assumptions.

It is assumed that the changeover circuit of Example #1 weighs 1 pound, and the paralleling and automatic protection circuits of Example #2 weigh 2 pounds. These are reasonable estimates for the simplest kind of equipment, usable up to about 10KVA system power ratings.

The power level of the system is assumed to be 3 kilowatts.

For the backup system of Example #1, the designer would be forced to use 3 inverters to meet the specified reliability. Each inverter would be rated 3KW.

In Example #2 four inverters are required, each rated 1.5KW.

Weight of standby type system:

From Figure 59, each inverter weighs 64 pounds.

Changeover circuit weight = 2 x 1 lb. = 2 lbs.

Total weight = 3 x 64 + 2 = 194 lbs.

Weight of parallel type system:

Each inverter weighs 42 pounds.

Each paralleling circuit weighs 2 pounds.

Total weight = 4(42 + 2) = 176

Weight saving = 18 lbs. = 9.3%

The preceding examples illustrate one of the advantages of paralleling inverters; weight may be saved by tailoring the system to the reliability requirements. It is a general rule that increasing reliability by redundancy always results in higher weight. This is true in parallel systems, as well as standby type systems. The advantage of paralleling is that the designer is not forced to accept a higher reliability and weight than is actually required. Because the weight of the paralleling circuits is not a function of rating, more weight will be saved as system power rating goes above 3KW. Furthermore, the reliability of the individual inverters used in a parallel system may actually be higher than the reliability of the standby type units, because the lower power rating allows the use of fewer parts in the parallel units. Hence, the potential weight saving may be greater than example indicates.

To help determine the number of inverters that should be used in a redundant system the following two general rules are helpful. First, reliability is increased by allowing a greater fraction of the total number of inverters to be potential failures. For example, allowing for two out of four failures will give greater system reliability than allowing for one out of four. Second, given a certain fraction allowed to fail, greater reliability results from using more units in the system. For example, a system having 6 inverters of which three may fail, is more reliable than a system having 4 inverters of which two may fail. Minimizing system weight is a matter of finding the combination having the smallest total number of units, that will just meet the specified reliability.

There are several other factors involved in parallel inverter system design, some of which are undoubtedly of greater importance than the potential weight reduction.

It will be recalled that in the examples it was assumed that the MTBF's of the various system components were known, through calculations. While convenient for illustrative purposes, such an assumption does not reflect a typical situation. Reliability calculations depend on empirical data, which are never as complete as one would like. Electrical parts are tested, under various conditions, and reliability predictions are made on the basis of the data that are gathered. However, the test conditions rarely duplicate the exact conditions encountered in actual use.

Frequently, a new design demands parts for which no reliability test data are available. In these cases, the reliability analyst is forced to estimate the parts' reliability, based on data for similar parts tested in the past. The accuracy of such estimates is not known. For these reasons, the accuracy of a reliability analysis performed on as complex a piece of equipment as a new inverter design is always open to question.

Equipment frequently fails prematurely because certain electrical or environmental conditions were not foreseen during the design and thus, were not accounted for in the reliability analysis. Often, such failures do not occur until after the equipment has been tested and placed in service. Obviously, the way to avoid such troubles is to gain field experience, analyze failures and modify the design until adequate reliability is achieved. This is where the ability to parallel inverters can be very advantageous. In a parallel system, older more refined inverter designs can be used, and the system reliability can be predicted with confidence. Higher power systems would simply use a larger number of inverters. By contrast, the standby type of system would probably require a new inverter design for each new power level, resulting in lower reliability, less confidence in the reliability prediction, and higher cost as well.

It is not meant to imply that, if paralleling were an accomplished fact, no new designs would ever be required. But the number of new designs could certainly be reduced, and new designs could be brought forth at a more relaxed pace, in keeping with advances in material and component technology. Also, the system designer would have available better design information and have it sooner.

The ability to reach high power levels is another advantage of paralleling. As space technology advances, the electrical power requirements of vehicles will almost surely increase. However, the maximum power that can be delivered by a single static inverter is limited by the power rating of the electrical parts, such as transistors, available at the time the inverter is designed. Of course, paralleling of load-carrying elements within the inverter offers greater

power capacity, but at the expense of efficiency. Internal paralleling always tends to reduce efficiency. This effect becomes more pronounced as the number of parallel elements increases.

Paralleling of whole inverters is free of these defects. The inverters will operate at normal efficiency and temperature, while the paralleling circuits consume very little additional power. Furthermore, the presence of several inverters in the system allows for a considerable increase in reliability, much better than a single inverter using paralleled elements.

The parallel redundant system offers the advantage of a higher overload capacity than the standby redundant system, during the early stages of the mission while all the inverters are still operating. This can be an advantage, for instance, where the load includes induction motors requiring high starting currents.

Another potential advantage of parallel inverter systems is that a continuous flow of power may be maintained, even if one inverter should fail. This is in contrast to the standby type of system, in which the functioning of the change-over circuits will cause a momentary loss of power, perhaps detrimental to the load equipment.

Figure 61 summarizes the major points covered in this part of the report. It shows the relative advantages of each of the three approaches.

The parallel inverter system offers the most flexibility and the highest potential power capacity of the three approaches discussed. The reliability and weight may be traded off to effect a suitable compromise for each application.

Type of System	Single Inverter	Standby Redundant	Parallel Redundant
Reliability	Inadequate for extended missions	Improves in discrete steps as more units are added	Any specified reliability may be met precisely
Weight	Lightest weight per unit power	Weight depends on reliability	Weight depends on reliability
Maximum Power	Limited by components	Limited by components	Unlimited - Any number of units may be paralleled
Complexity	Simplest	Complex	Most complex
Result of Failing One Inverter	Permanent loss of power	Momentary loss of power	No loss of power

Figure 61. Comparison of Inverter Systems

V. TRANSFORMER IMPROVEMENT EVALUATION

Two inverter output transformers were assembled for evaluation and are shown in Figure 62. As described in the first quarterly report, one transformer uses conventional singly-oriented silicon-iron core material, 0.011" thick Hipersil steel. The other transformer uses a new doubly-oriented field-annealed silicon-iron core material, known by the Westinghouse trade name of CUBEX. Equal cross-sectional areas of iron were used in each transformer core. Each transformer weighs approximately 7.2 pounds. The annealing processes used for both the Hipersil steel and CUBEX steel transformer laminations are described in Appendix IV.

These two transformers were first evaluated with sinusoidal excitation voltage and then operated individually in the same static inverter test model.

A. Characteristics of Transformer Cores with 400 cps Sinusoidal Excitation Voltage.

To obtain core loss and a-c excitation data from a magnetic core material, it is desirable to have a perfectly uniform cross sectional area throughout the entire magnetic path. This facilitates the calculation of the operating flux density and the core weight. These conditions were approached with the inverter output transformers by placing a shorted turn around each of the four interior core legs to prevent flux from passing through these sections of the core. Then 400 cps flux was caused to follow the outside core legs by applying 400 cps sinusoidal voltage to the four primary windings connected in series. Voltage was applied to only half of each 90-turn primary winding, making a total effective winding of 180 turns.

The effective cross sectional area of the outside core legs was determined by measuring the stack height on each transformer and determining the product of the stack height, known width (0.545"), and the stacking factor (0.95 for 0.011" Hipersil steel laminations and 0.90 for 0.006" CUBEX steel laminations). The measured stack height was 0.964" for the CUBEX steel transformer and 0.909" for the Hipersil steel transformer. The effective cross sectional area for each core is therefore 0.47 in^2.

The flux density B is a function of the applied voltage according to the following equation:

$$B = \frac{V \times 3.49 \times 10^6}{A \times f \times t} \text{ gauss}$$

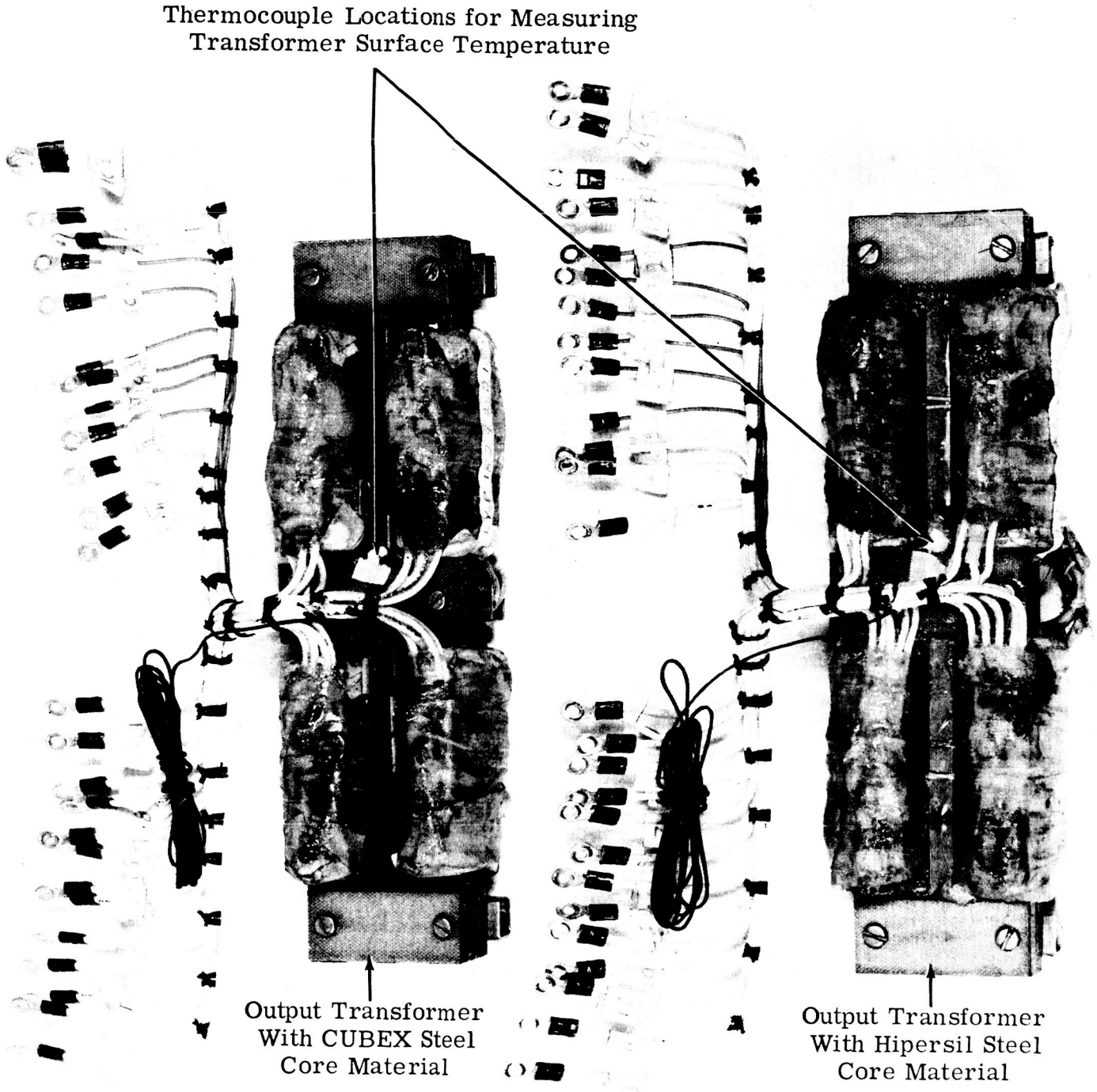


Figure 62. Static Inverter Output Transformer Models Used in the Transformer Improvement Evaluation

where V = applied a-c 400 cps volts RMS

A = effective core cross sectional area; 0.47 in^2

f = frequency of applied voltage; 400 cps

T = 180 turns

By substitution:

$$B = \frac{V \times 3.49 \times 10^6}{0.47 \times 400 \times 180} = 103\ V \text{ gauss}$$

By referring to the lamination dimensions given in the first quarterly report, the volume of iron in the outside core legs was calculated and found to be 10.6 cubic inches. Using the known material density of 0.255 pounds-per-cubic inch, the weight of the core which was excited in this test is 2.7 pounds.

The accurate measurement of core loss and a-c excitation is a difficult task because the excitation current becomes non-sinusoidal as the core begins to saturate. Conventional 0.25% Westinghouse or Weston wattmeters will not give accurate indications when the applied currents have high harmonic content. To avoid these problems, test data were obtained using a VAW Meter which is manufactured by the John Fluke Engineering Company. This meter has an accuracy of ±3% over a frequency range of 20 to 20,000 cps. The recorded test data for both transformers are given on the following two pages, Figures 63 and 64. The winding resistances were measured and the copper loss was subtracted from the measured loss to obtain the core loss for a variety of excitation levels. The core loss in watts-per-pound, the core a-c excitation in apparent watts-per-pound, and the flux density in kilogauss were calculated from these test results and plotted for comparison in Figures 65 and 66.

At the designed operating flux density of 13 Kg the CUBEX steel core had a loss of 7.7 watts-per-pound compared with 11.6 watts-per-pound for the Hipersil steel core. At this same flux density, the CUBEX steel core required 13.3 volt-amperes excitation per pound compared with 21.5 volt-amperes excitation per pound for the Hipersil steel core. The use of 0.006" CUBEX steel laminations represents a 33% reduction in core loss and a 38% reduction in required excitation when compared with 0.011" Hipersil steel laminations. This reduction is even more significant at higher flux densities.

The total used core weight, including the internal core legs, is 3.3 pounds. Therefore, when the transformer is operated at 13 Kg, the difference in core loss for the two materials should be $(11.6 - 7.7) \frac{\text{watts}}{\text{pound}} \times 3.3$ pounds = 12.8 watts. This can be expected to change the efficiency of the 750 VA inverter model by approximately $\frac{12.8}{750} \times 100\% = 1.7\%$.

K 166091

SUBJECT INVERTER/CONVERTER LYP18293J1

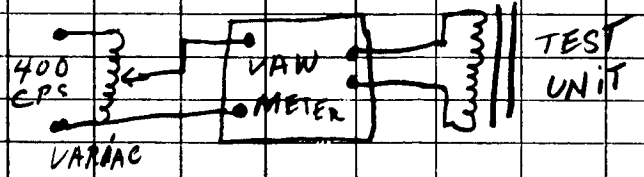
CUSTOMER ENGRG. DEPT. SERIAL NO. LYP18293-D4

S. O. OR TEST NO. N4-202 D. OR L. SPEC. NO. EIN-5J - SHAFT NO. LYP18292 FRAME NO.

TO DETERMINE CORE LOSS OF TRANSFORMER

A.C. VOLTS	A.C. AMPS	AC WATTS	COPPER LOSS I^2R	CORE LOSS WATTS
20	.05	.9	<0.1	.9
40	.09	3.2	<0.1	3.2
60	.125	6.6	<0.1	6.6
80	.17	11.5	<0.1	11.5
100	.231	17.5	<0.1	17.5
120	.39	27.0	<0.1	27.0
140	.825	46.0	.29	45.71
150	1.21	60.0	.597	59.4
160	2.2	95.0	1.9	93.1
170	3.28	130.	4.3	125.7
180	5.0	170	10.2	159.8
190	12.5	500	64.4	435.6

POWER APPLIED TO TRANSFORMER LEADS 1 & 23, WITH LEAD 10 CONNECTED TO LEAD 13, LEAD 3 CONNECTED TO 7, AND LEAD 15 CONNECTED TO LEAD 21. 1 SHORTED TURN PLACED AROUND EACH INTERIOR CORE LEG. PRIMARY RESISTANCE = .408 Ω



JOHN FLUKE ENGR. CO. MODEL 103 VAW METER Ser #4

PREVIOUS TEST PAGE 3-18-64 DATE R. Marker - A. Stevenson SIGNED G. ERNSBERGER ENGINEER IN CHARGE

Figure 63. Measured Core Loss and A-C Excitation for Hipersil Steel Core with 400 cps Sinusoidal Excitation Voltage

K166915

SUBJECT INVERTER / CONVERTER P/N LYP18293-J1

CUSTOMER ENGRG DEPT. SERIAL NO. LYP18292-D1

S. O. OR TEST NO. N4-[illegible] D. OR L. SPEC. NO. EJN-5J- SHAFT NO. LYP18292 FRAME NO.

TO DETERMINE CORE LOSS OF TRANSFORMER

AC VOLTS	AC AMPS	AC WATTS	COPPER LOSS I²R	CORE LOSS WATTS
20	.045	1.44	<0.1	1.44
40	.075	2.7	<0.1	2.7
60	.095	5.4	<0.1	5.4
80	.135	9.4	<0.1	9.4
100	.18	13.9	<0.1	13.9
120	.27	19.5	<0.1	19.5
140	.312	25.0	<0.1	25.0
150	.388	29.0	<0.1	29.0
160	.65	36.5	.17	35.33
170	.975	50.0	.39	49.71
180	1.8	72.0	1.3	70.7
190	4.4	110.	7.9	102.1
197	10.75	310.	47.5	262.5

POWER APPLIED TO TRANSFORMER LEADS 1 & 23 WITH LEAD 10 CONNECTED TO LEAD 13, LEAD 3 CONNECTED TO 7 AND LEAD 15 CONNECTED TO LEAD 21.

1 SHORTED TURN PLACED AROUND EACH INTERIOR CORE LEG.

PRIMARY RESISTANCE = .41 Ω

JOHN FLUKE MODEL 103 VAW METER Ser #4

SEE PAGE K166917 FOR TEST SET-UP

PREVIOUS TEST PAGE 3-19-64 DATE K. Marker - A. Stevens SIGNED G. ERNSBERGER ENGINEER IN CHARGE

Figure 64. Measured Core Loss and A-C Excitation for CUBEX Steel Core with 400 cps Sinusoidal Excitation Voltage

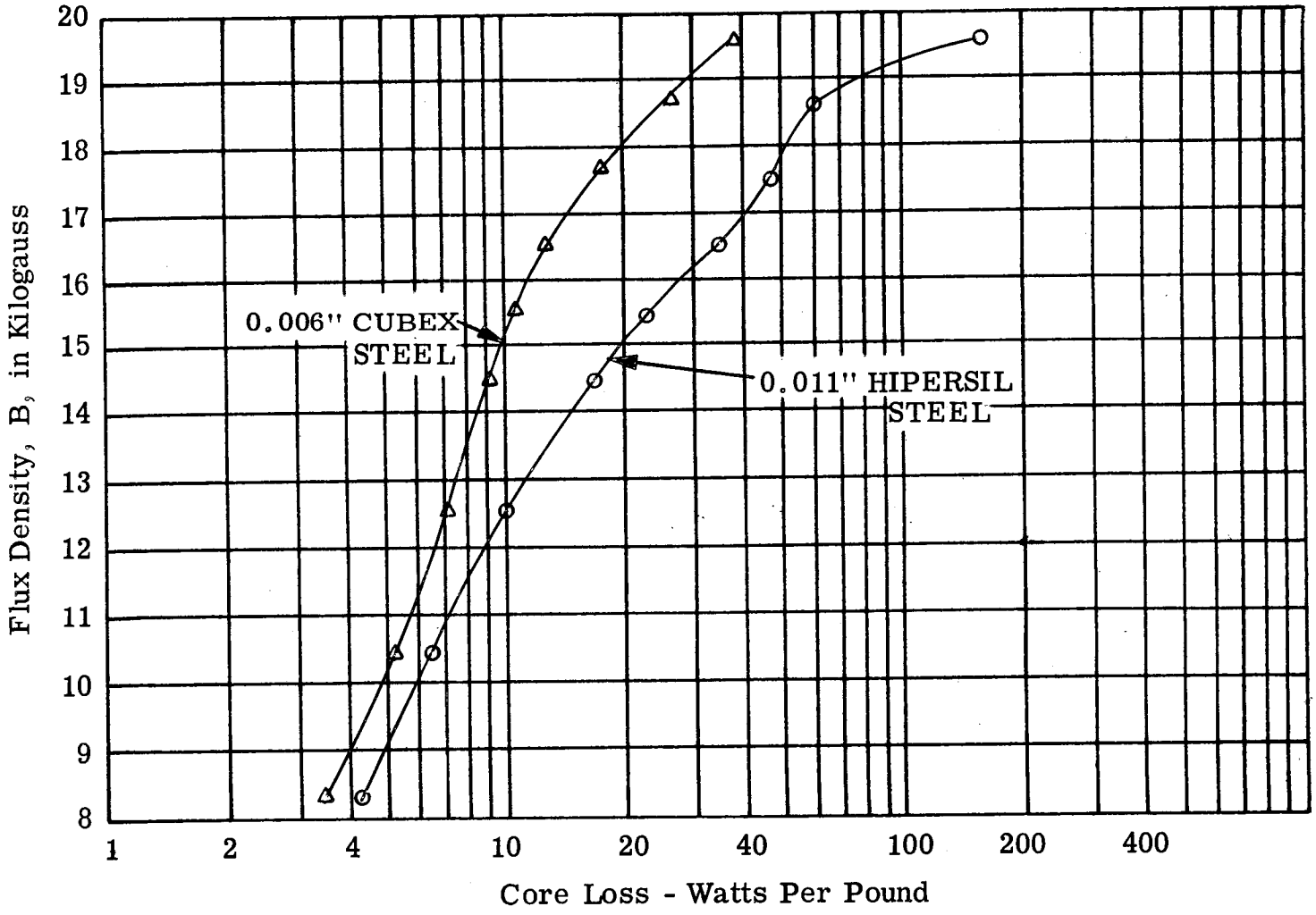


Figure 65. A Comparison of Core Losses for CUBEX Steel and Hipersil Steel Transformer Cores with 400-cps Sinusoidal Excitation Voltage

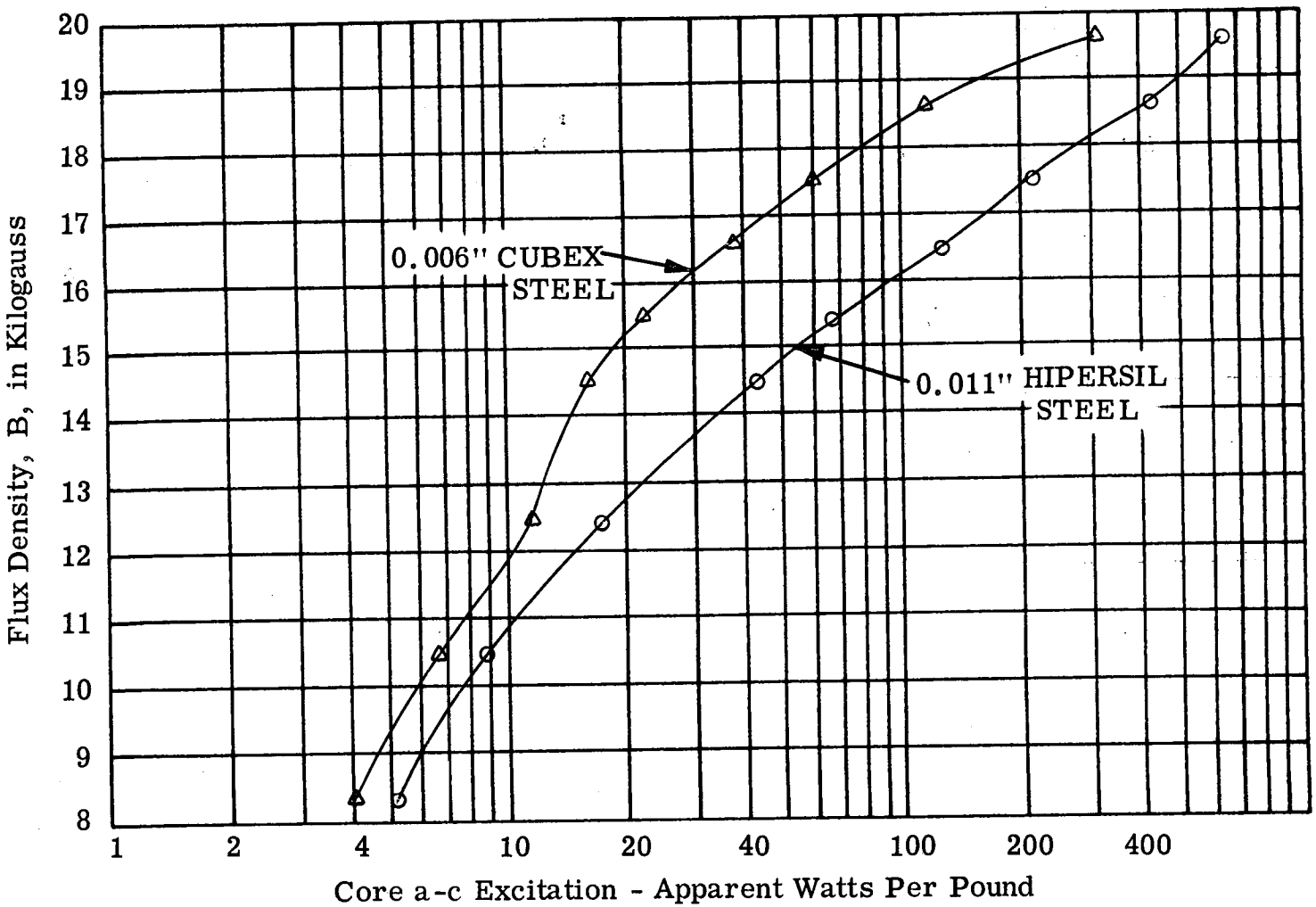


Figure 66. A Comparison of a-c Excitation for CUBEX Steel and Hipersil Steel Transformer Cores with 400-cps Sinusoidal Excitation Voltage

It should be noted that about half of the improvement in core material characteristics is a result of the difference in material thickness. This is illustrated in Figure 1 of the first quarterly report.

B. Effect of Transformer Core Material on Static Inverter Efficiency.

Tests were conducted in accordance with Section 7 of the laboratory test specification (see Appendix I) to determine the inverter efficiency with each different transformer installed. Inverter efficiency was determined with loads ranging from 25 to 125 percent of full load and with power factors ranging from 0.75 lagging to 0.9 leading. Actual test data are recorded in Figures 67 and 68. Wattmeter and voltmeter potential coils presented an additional 12 watts load to the inverter and has been included in the efficiency calculations.

The test results are plotted in Figures 69 through 72. The inverter efficiency improved under all load conditions through the use of the CUBEX steel transformer. Efficiency improvement at full load ranged from as low as 1.0% to as high as 2.6%. This wide range is expected because the transformer core flux density changes as the load power factor changes; also, the anticipated savings in core loss of 12.8 watts is 1.7% of full load watts at unity power factor but is 2.3% of full load watts at 0.75 power factor. The improved efficiency of the inverter is caused directly by the reduced core loss of the CUBEX steel output transformer. This increase in efficiency was possible without increasing the transformer or inverter weight.

During the transformer evaluation, the surface temperature of the transformers was allowed to stabilize at zero load and at full load, unity power factor. The surface temperature was measured at the top center portion of the core with thermocouples located as shown in Figure 62. The zero and full load temperature rose to 82.5 and 120°C respectively for the Hipersil steel transformer. The zero and full load temperature rose to 66 and 101°C respectively for the CUBEX steel transformer. Normal room temperature conditions (25°C) prevailed during the test. This lower temperature rise adds to the life of electrical insulation and could be important on extremely long duration applications.

C. Effect of Transformer Core Material on Static Inverter Weight.

In some applications it may be more desirable to reduce the weight of the static inverter than to increase efficiency. The improved magnetic characteristics of the CUBEX steel alloy allow the transformer designer to reduce the weight of a transformer without changing its efficiency.

K166915

SUBJECT INVERTER/CONVERTER P/N LYP1129351

CUSTOMER ENGR. DEPT. SERIAL NO. B. B. #2 TRANSFORMER

S. O. OR TEST NO. N4-202 ~~S. OR L.~~ SPEC. NO. E2-N-5J ~~SHAFT~~ NO. LYP8293 ~~FRAME~~ NO. P/N LYP1129304

TO DETERMINE COMPARISON BETWEEN CONVENTIONAL CORE MATERIALS AND "CUBEX" CORE MATERIAL IN OUTPUT TRANSFORMER 7.1#

PARA. 7.0 SINGLE INVERTER.

		STAB.				STAB.							
#2	V1-N	115.2	114.0	113.8	113.5	113.7	112.5	115.5	114	114	115.2	115.5	111.5
#2	V2-N	115.0	114.0	113.5	113.5	113.5	112	115.0	113.8	113.5	113.0	114	109.5
#2	V3-N	114.0	113.0	113.0	113.2	114	113	114.3	113.8	114.5	115.2	115.0	112
#2	A1	0	.55	1.08	1.63	2.2	2.74	0	.55	1.1	1.66	2.18	2.73
#2	A2	0	.50	1.05	1.59	2.16	2.74	0	.52	1.09	1.62	2.12	2.68
#2	A3	0	.50	1.05	1.6	2.17	2.76	0	.52	1.09	1.65	2.15	2.72
#2	W1	0	62.5	125	188	250	312	0	46	94	145	186	234
#2	W2	0	62.0	123	186	253	313	0	49	92	142	181	227
#2	W3	0	59.0	119	182	254	319	0	46	93	144	189	238
#2	DC-IN AMPS	3.6	10.9	19.0	28.0	39.5	50.0	3.7	9.5	15.5	23.5	29.8	37.8
#2	DC-IN VOLTS	30.1	29.7	29.2	28.6	28.0	27.2	30.1	29.8	29.4	28.9	28.3	27.9
%	LOAD	0	25	50	75	100	125	0	25	50	75	100	125
	PF	-	1.0	1.0	1.0	1.0	1.0	.75	.75	.75	.75	.75	.75
*	TC Eff C	82.5	60.4%	68.3%	71.0%	69.5% 120	70.3%		54.0%	63.9%	65.0%	67.3%	67.3%

* NOTE: THERMOCOUPLE LOCATED ON THE IRON OF THE MIDDLE CORE STACK NEAR THE CENTER OF TRANSFORMER

#2	V1-N	115	114	114	114	115.	112	115.2	115.5	115.	113.	112.	111.
#2	V2-N	114.8	113.8	113.5	113.5	113.5	110.5	115.	115.5	112.5	115.	115.	112.
#2	V3-N	114	113.8	114.	114.2	115.	112.8	114.	112.0	114.	112.5	115.5	113.
#2	A1	0	.55	1.1	1.65	2.19	2.75	0	.55	1.1	1.63	2.15	2.72
#2	A2	0	.55	1.05	1.6	2.15	2.72	0	.55	1.05	1.63	2.2	2.7
#2	A3	0	.55	1.08	1.62	2.19	2.76	0	.6	1.05	1.65	2.18	2.73
#2	W1	0	56	113	170	225	283	0	55	120	175	226	282
#2	W2	0	56	112	165	220	275	0	59	114	176	235	285
#2	W3	0	55	110	167	224	284	0	56	112	169	223	283
#2	DC IN AMPS	3.6	10.5	17.7	26.5	35.0	44.0	3.7	10.6	18.5	27.0	36.0	45.8
#2	DC-IN VOLTS	30.1	29.7	29.1	28.6	28.1	27.5	30.1	29.7	29.2	28.6	28.0	27.5
%	LOAD	0	25	50	75	100	125	0	25	50	75	100	125
	P.F.	.9 LAG	.9 lag	.9 lag	.9 lag	.9 lag	.9 lag	.9 LEADING	.9 lead	.9 lead	.9 lead	.9 lead	.9 lead
	Eff.		57.4%	67.4%	67.8%	69.2%	70.6%		57.8%	66.3%	68.9%	69.0%	68.4%

PREVIOUS TEST PAGE

3-18-64 DATE

Marker - Stevenson SIGNED

G. ERNSBERGER ENGINEER IN CHARGE

Figure 67. Inverter Efficiency Measurements with the Hipersil Steel Output Transformer Installed

K166091o

SUBJECT INVERTER/CONVERTER P/N LYP 18293-51

CUSTOMER ENGR. DEPT. SERIAL NO. B.B. #2 TRANSFORMER

S. O. OR TEST NO. N4-202 SPEC NO. E2N-5I SHAFT NO. LYP 18293 FRAME NO. P/N LYP 18292 B1

TO DETERMINE COMPARISON BETWEEN CONVENTIONAL CORE MATERIALS AND "CUBEX" CORE MATERIALS IN OUTPUT TRANSFORMER. 7.36 #

PARA. 7.3 SINGLE INVERTER

		STAB				STAB								
#2	V1-N	115	114	114	113.3	113.2	112		115	114	113.5	113.5	113.5	111.5
#2	V2-N	115	113.8	113.8	113.8	113.	113		115	113.7	113.2	113.2	113.5	111.5
#2	V3-N	114.5	113.5	113.2	113.3	114	113.5		114.7	113.5	114	114	114.5	113.
#2	A1	0	.55	1.09	1.63	2.19	2.75		0	.55	1.1	1.65	2.2	2.71
#2	A2	0	.51	1.06	1.61	2.16	2.75		0	.53	1.07	1.63	2.17	2.7
#2	A3	0	.51	1.07	1.6	2.16	2.74		0	.53	1.05	1.65	2.2	2.73
#2	W1	0	61	125	187	250	314		0	47	95	142	189	226
#2	W2	0	60	124	188	255	316		0	47	96	142	184	230
#2	W3	0	59	119	183	252	315		0	45	94	141	185	232
#2	DC IN AMPS	3.1	10.3	18.3	27.	38.5	49.5		3.3	8.9	14.8	21.7	28.3	35.
#2	DC IN VOLTS	30.1	29.7	29.1	28.5	28.0	27.3		30.1	29.9	29.5	29.	28.6	28.2
%	LOAD	0	25	50	75	100	125		0	25	50	75	100	125
	PF	1.0	1.0	1.0	1.0	1.0	1.0		.75	.75	.75	.75	.75	.75
*	TC- °C EN	66°C	62.8%	71.4%	74.1%	71.3% 101°C	70.8%			56.7%	68.0%	69.5%	69.7%	70.9%
#2	V1-N	115	114.2	113.5	113.5	113.5	111.5		115	111.5	113.5	113.5	112.5	111.
#2	V2-N	115	113.8	113.2	113.5	114	112.		115	115.	115.	114	116.	113.2
#2	V3-N	114.5	113.5	113.8	114	114.5	113.2		114.5	114.	113.	113	113.5	113
#2	A1	0	.53	1.1	1.65	2.17	2.72		0	.52	1.07	1.65	2.14	2.73
#2	A2	0	.51	1.08	1.63	2.16	2.72		0	.5	1.08	1.63	2.22	2.69
#2	A3	0	.51	1.07	1.65	2.16	2.73		0	.53	1.05	1.61	2.17	2.73
#2	W1	0	56.	111	169	225	284		0	54	115	174	225	282
#2	W2	0	56.	111	169	226	285		0	57	118	175	240	287
#2	W3	0	55.	109	167	225	286		0	55	116	166	222	282
#2	DC IN AMPS	3.3	9.9	16.5	25.	34.1	43.1		2.2	10.2	18.0	26.6	35.7	45.5
#2	DC -IN VOLTS	30.1	29.8	29.4	28.7	28.1	27.6		30.1	29.7	29.2	28.6	28.	27.4
%	LOAD	0	25	50	75	100	125		0	25	50	75	100	125
	PF	.9lag	.9lag	.9lag	.9lag	.9lag	.9lag		.9led	.9led	.9led	.9led	.9led	.9led

* NOTE: THERMOCOUPLE LOCATED ON THE IRON OF THE MIDDLE CORE STACK NEAR THE CENTER OF TRANSFORMER

Eff %	60.7%	70.6	72.0	71.8	73.0		58.8	67.5	69.3	70.0	69.2

PREVIOUS TEST PAGE

3-18-64 DATE R. Marker - A. Steinmann SIGNED C. ERNSBERGER ENGINEER IN CHARGE

Figure 68. Inverter Efficiency Measurements with the CUBEX Steel Output Transformer Installed

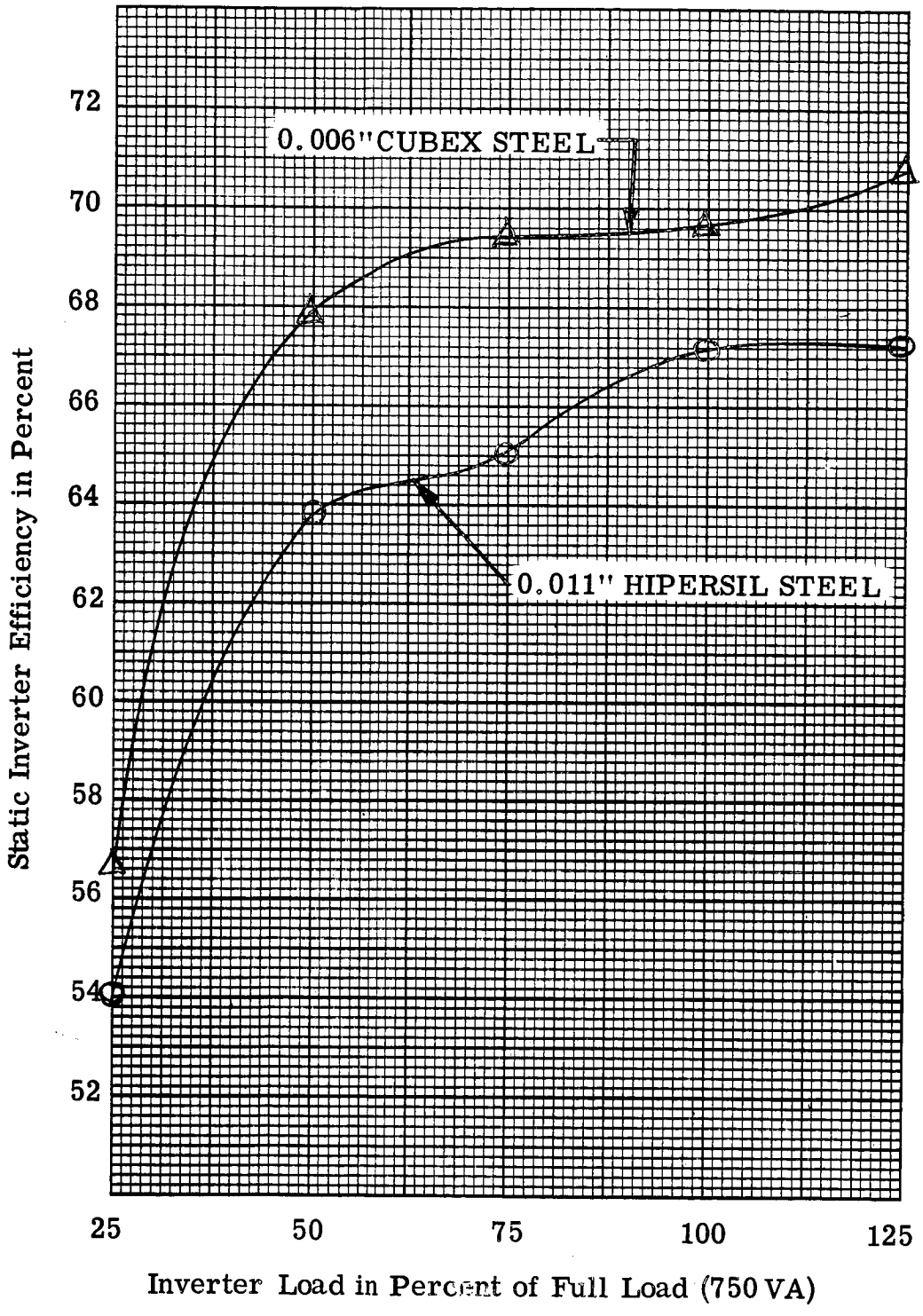


Figure 69. The Effect of Output Transformer Core Material on Inverter Efficiency for 0.75 Lagging Power Factor Loads

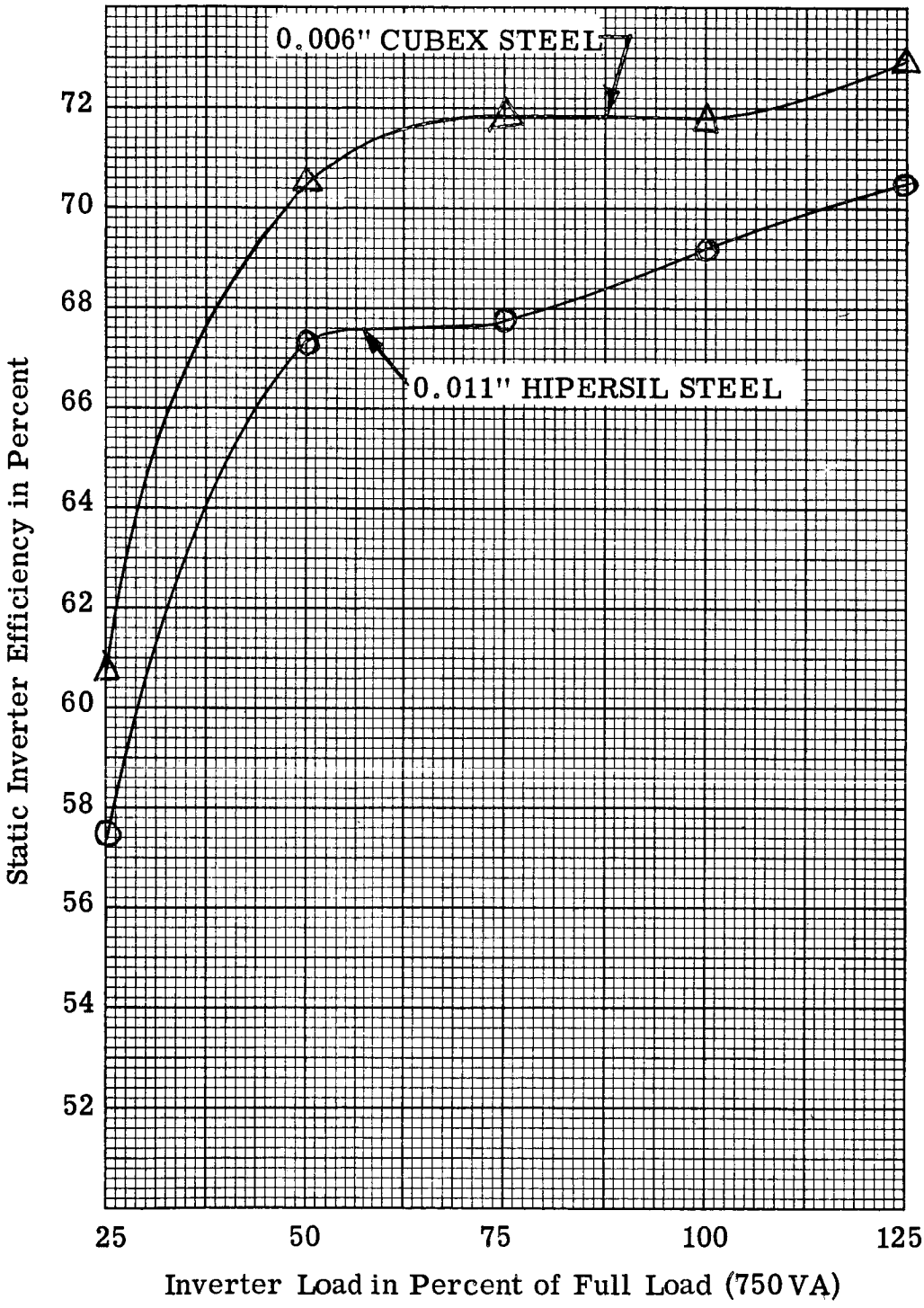


Figure 70. The Effect of Output Transformer Core Material on Inverter Efficiency for 0.9 Lagging Power Factor Loads

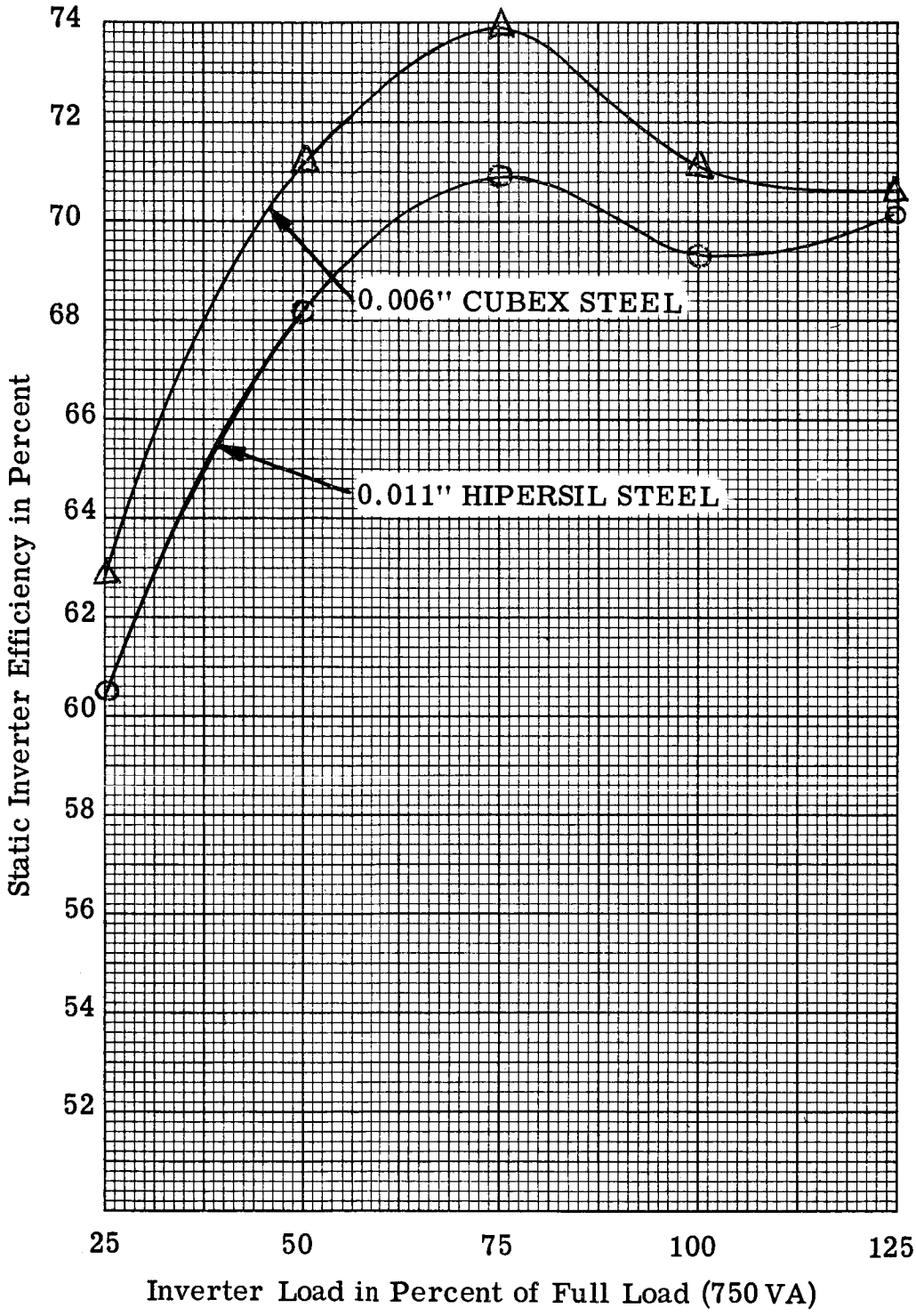


Figure 71. The Effect of Output Transformer Core Material on Inverter Efficiency for 1.0 Power Factor Loads

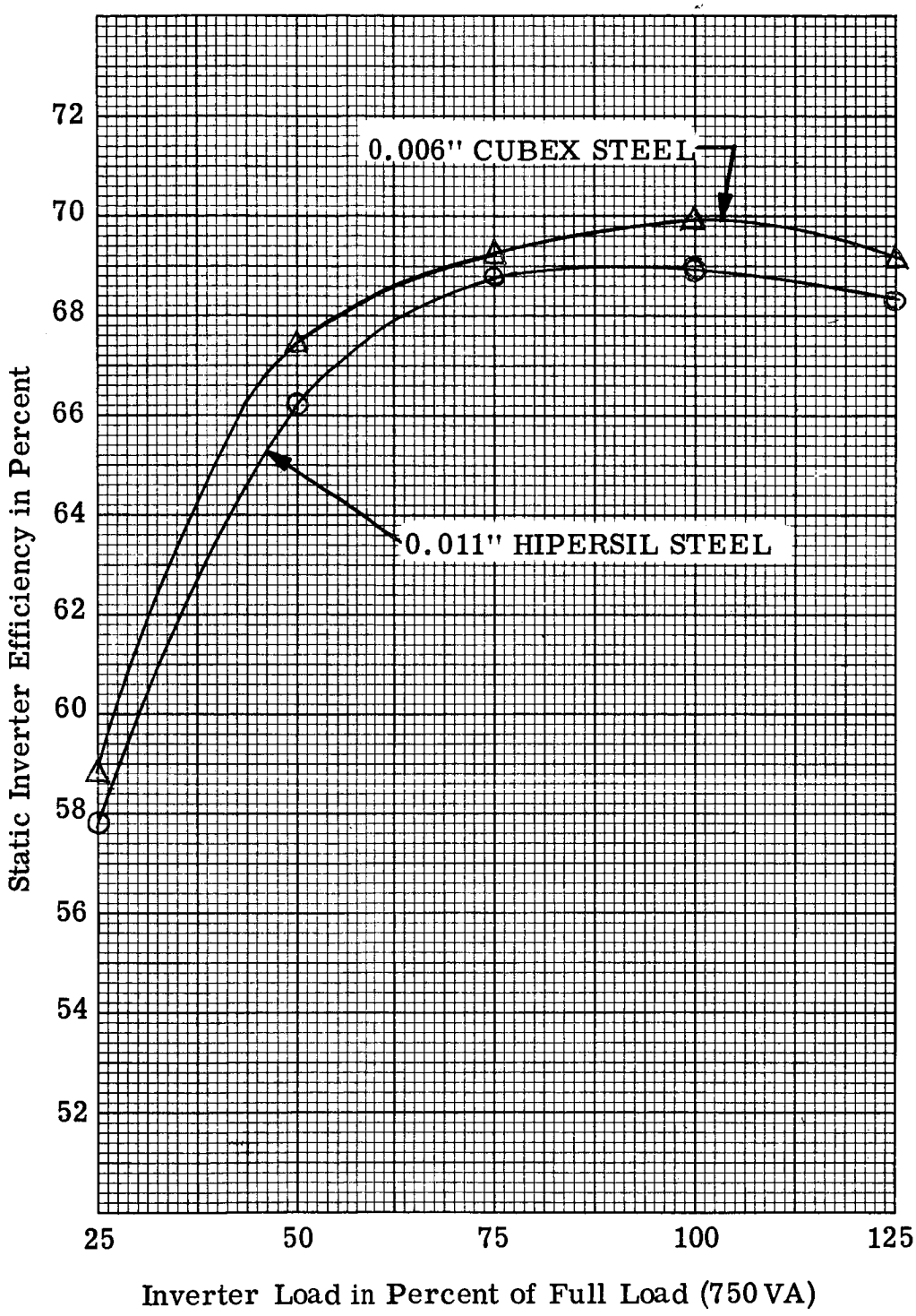


Figure 72. The Effect of Output Transformer Core Material on Inverter Efficiency for 0.9 Leading Power Factor Loads

To illustrate the magnitude of the weight reduction that is possible, refer to Figure 65. Based on this comparison of core losses, CUBEX steel alloy can be operated with a flux density of 16 kilogauss and have the same loss as Hipersil operating at 13 kilogauss. The a-c excitation is practically the same at these two operating conditions. For example, a CUBEX steel alloy transformer will weigh approximately 13/16th as much as a Hipersil steel transformer having equal efficiency. The two transformers used in this evaluation weigh approximately 7.2 pounds apiece. The reduction of (1-13/16) 7.2 pounds = 1.3 pounds represents a 19% reduction in transformer weight with no increase in losses.

The inverter models which were used in this evaluation have a packaged weight of 26 pounds. By using a CUBEX steel alloy output transformer, this packaged weight could be reduced by 1.3 pounds without reducing efficiency. This represents a 5% savings in inverter weight.

VI. PLANS FOR FUTURE WORK

The scope of this contract has been extended five months to include the following additional tests:

(1) Design and build circuits which will efficiently and reliably provide automatic paralleling and protection for two or more static inverters or converters.

(2) Design the necessary components and devices to be used with or in the automatic circuits.

(3) Demonstrate the operation of the automatic paralleling and protection systems with the two existing inverter and converter models.

(4) Additional testing and evaluation will be done to determine the automatic performance characteristics of the paralleled inverter and converter systems.

VII. CONCLUSIONS

This report contains (A) the results of the laboratory evaluations of the static inverter and converter paralleling circuits, (B) the results of the laboratory evaluation of the CUBEX steel output transformer, and (C) a study of the weight reduction and reliability improvements made possible by operating static inverters or converters in parallel. The conclusions in these areas will be listed separately.

A. Static Inverter and Converter Paralleling Circuits.

1. Parallel Inverter Evaluation.

The results of the laboratory evaluation of the static inverter paralleling circuits show that static inverters can be satisfactorily paralleled if the necessary conditions are satisfied. Those conditions are described, in detail, in the first quarterly report. Briefly they are: (a) all inverters must operate at exactly the same frequency, (b) the internal voltage of all inverters must be in phase with each other at all times, (c) all nominal regulated output voltages shall be the same and (d) each inverter must have provisions to insure proper load division.

The frequency locking circuit, described in the first quarterly report, operated properly after a slight circuit modification. This frequency locking circuit is essentially a bi-stable circuit which allows only one frequency standard to operate at a given time. This frequency locking circuit can be eliminated if only one frequency standard is used for a parallel system. This approach is recommended and will be followed during the remainder of the contract. Each inverter will have a unijunction-transistor-oscillator as a secondary frequency standard which will be synchronized with one primary frequency standard prior to connecting the inverters in parallel.

The phase locking circuits also operated properly. However, the operation of the phase locking circuits causes a one cycle transient to appear at the output terminals of one or both of the inverters. This one cycle transient may be detrimental to some loads and can be eliminated if the frequency locking circuits are energized at an instant when the countdown circuits of both inverters are in phase. This procedure is recommended and will be incorporated into the automatic paralleling circuit which will be developed during the remainder of this contract.

The actual gain of the load division circuits was 9.5% higher than the design gain. The actual load division between paralleled inverters was much better than predicted by the design procedure outlined in the first quarterly report. The test results demonstrated conclusively that both real and reactive load can be divided satisfactorily between paralleled static inverters. Any reasonable load division requirement can be met and any number of inverters can be operated in parallel with this method.

2. Parallel Converter Evaluation.

The laboratory evaluation of the static converter paralleling circuits shows that static converters can be operated in parallel if the necessary conditions are met. Those conditions are: (a) the converters must have the same nominal regulated output voltage, and (b) have provisions in each voltage regulator circuit to cause the converters to share load current.

The converter load division circuit described in the first quarterly report did not operate properly for reasons discussed in this report. A modified load division circuit was designed, incorporated into the two static converter models, and gave very satisfactory load current division during the laboratory evaluation. This converter load division method is adaptable to a wide range of converter output voltages and currents and can be designed to give any desired load division accuracy. Any number of converters can be operated in parallel with this method.

It was necessary, in the test model converters, to filter the converter output voltage to eliminate a low-frequency output-voltage-amplitude modulation which occurred during parallel operation. This voltage-amplitude modulation was caused by the slight frequency difference between the two tuning fork oscillators used as frequency references in the inverter portions of the test models. This output voltage filtering may not be necessary in converters which obtain a d-c output voltage by rectifying a square-wave voltage.

B. Transformer Core Evaluation.

The effect of using field-annealed doubly-oriented CUBEX steel core material in place of singly-oriented Hipersil steel core material was determined by laboratory evaluation. CUBEX steel has lower losses for a given flux density that does Hipersil steel. When both cores were operated at 13 kilogauss the CUBEX steel core had 33% lower core loss and 38% lower excitation required than did the Hipersil steel core. The weight of the CUBEX steel core could have been reduced by 19% to obtain the same core loss that the

Hipersil steel core had at 13 kilogauss. Approximately half of the material improvement noted above is a result of the fact that the CUBEX steel laminations were 0.006" thick and the Hipersil steel laminations were 0.011" thick. However, the use of CUBEX steel still offers significant improvements in weight and/or efficiency.

C. Weight Reduction and Reliability Improvement Study.

Three different static inverter power system approaches were considered in this study. Those approaches were (1) single inverter system, (2) standby inverter system, and (3) parallel inverter system. The study shows that the parallel inverter system offers the most flexibility and the highest potential power capacity of the three approaches. The reliability and weight of a parallel inverter system may be traded off to effect a suitable compromise for each application. The single inverter system is considered unsatisfactory for extended missions.

APPENDIX I

LABORATORY TEST SPECIFICATION FOR TRANSFORMER AND PARALLELING EVALUATION

SM 11-61 LPLCO

SPECIFICATIONS FOR LABORATORY TEST NO. N4-202

☐ Dept. 81. (Engr. to send all four copies to lab.) Lab. adds cost and schedule and returns 2 copies to:

☐ _____ Engr. Dept.—Eng. Dept. clerk distributes:

☐ 1 copy to Section File ☐ 1 copy to Engr. Mgr.

FILE—Del. Fol. Section after above is crossed out.

APPARATUS: (2) Inverter/Converter Models (P/N LYP18293J1 and (1) Transformer (P/N LYP18292D1)

OBJECT: (1) To demonstrate feasibility of paralleling inverters & converters. (2) To evaluate performance of a transformer utilizing field annealed doubly oriented silicon-iron in an inverter circuit and compare results with those of conventional transformer core materials.

20006-1B
Scheduled SE/PE 20006-2B Priority _____

Trouble Docket or Development Project No. _____

Sample LY P18292 & 3 Charge See Below

Test LY _____ Eng. Test _____

Hours _____ $ _____ Start _____ Cpt. _____

Frame/Type _____ Rotation _____ (End opposite shaft)

P/N _____ G. O. CLD 22790

Customer _____

Style _____ Section _____

OUTLINE _____ Line Wiring Diag. _____ Diag. WAF _____ AC DC _____ Wd.

RATING _____ KW HP KVA _____ V _____ A _____ rated rpm. _____ max. rpm. _____ Ph. _____ Cy.

Res. _____ °C: Arm _____ Main Shunt _____ Aux. Series _____ Comp. _____ I.P. _____ Total Coil _____ Check and record all res.

Excitation _____ V _____ A. Brush Setting _____ (After running in brushes.)

Winding Off Neutral _____ bars CW. _____ CCW. _____ bars. Comm. Brake tests at fld. temp. _____ °C. Ground test 60 cy., 1 sec. _____ V.

Brushes: No. _____ Grade _____ Size _____ lg. _____ w. _____ tk. Dwg. _____ Ounces pressure _____

Ventilation: Self Forced Open Encl. _____ CFM. _____ inches water Dia. tube _____ Special Enclosure _____

Capacitor: _____ mfds. S No. _____ Thermoguard Spencer No. _____ Switch Op. Speed _____

Comm. test is/is not to be approved prior to curve test. Govt. witness test: USAF _____ USN _____ None _____

Test Specs. _____ Other test letters, on same unit or set-up _____

Record Data on Forms _____ Plot Curves _____ Check Weight _____

DISPOSITION AFTER TEST: Engineering Storeroom

INSTRUCTIONS and PROCEDURE: (Engineer to requisition all associated apparatus listed below. Laboratory to provide all test equipment required to perform tests.)

Sections 1, 2, 3, 4, and 5: (Charge E2N-5()-LYP18293)

Section 6: (Charge E2N-5()-LYP18292)

Signed G.W.Ernsberger G W Ernsberger Engineer—Date 1.10.64 Test No. N4-202

Approved R.L.Gasperetti Section Manager _____ Sub. _____

Test Equipment Required

No.	Description
2	0-32 volt, 35 amp, d-c power supply (E1, E2)
2	0-30 volt, d-c voltmeter
2	0-50 amp d-c ammeter
1	Oscilloscope, 10 Mc, dual channel
1	3 phase circuit breaker, 10 amps, 150 volts
2	DC vacuum tube voltmeters 0-30 volt
2	3 phase, 400 cps, 115V, 0-500VA/Ø, P.F. 0.9 leading to 0.5 lagging, load bank
2	0-150V a-c rms voltmeter
6	0-5 amp a-c ammeter
6	0-500 watt a-c wattmeter
2	Frequency counter
2	Selector switch box for voltmeters
1	Recording oscillograph
2	0-200V d-c voltmeter
2	0-10 amp, d-c ammeter
2	0-1000 watt d-c wattmeter

Unless otherwise specified instrument accuracy shall be as follows:

(a)	Frequency	±1 cycle
(b)	RMS voltage	±.25%
(c)	DC voltage	±.25%
(d)	RMS current	±.25%
(e)	DC Current	±.25%
(f)	Watts	±.25%

1.0 Measurement of Reactive Load Division Circuit Loop Gain.

Connect inverter model in test circuit described in Figure 73. Set input d-c voltage (E1) at 28 ± 1 volts.

1.1 Connect a three phase load on output terminals A2, B2, and C2 to N (Figure 8) such that the output load current is 1.0 PU, (2.18 amps/phase) .5 PF lagging. Measure the output voltages. These voltages should be 67.5 ± 10 volts rms line-to-neutral. Record the output voltages, currents and watts under this condition.

NOTE: The output voltage should decrease as the load current is increased. Therefore, the impedance of the load will have to be reduced accordingly to obtain 1.0 PU output current under these conditions.

2.0 Test of Frequency Lock Circuits.

2.1 Connect two inverters as shown in Figure 74. Do not connect d-c power supplies as shown in Figure 74. Open all switches. It is not necessary to connect the load nor output meters for this test of frequency lock circuits.

2.2 Disconnect d-c power from the power stages of the inverters.

2.3 Connect the + lead of a variable voltage d-c power supply through a switch to the input terminal (+INP). Use a separate d-c power supply for each inverter. Connect the negative lead of the d-c power supplies to (-INP) terminals.

2.4 Close switches K1, K2, and K3.

2.5 Connect a d-c vacuum tube voltmeter across the collector of transistor Q24 to (-INP) on each inverter. (These meters are indicators only and need not exceed ± 10% accuracy.)

2.6 Set the voltage on each d-c power supply at 28 ± 2 volts and apply d-c voltage to both inverters simultaneously.

2.7 One of the collectors of Q24 to (-INP) voltages should rise to 19 ± 1 volts while the other should rise to 3 ± 1 volts.

2.8 Connect a separate d-c power supply from base to emitter on Q25 on the inverter whose Q24 collector to (-INP) voltage is 3 ± 1 volts. Raise the base to emitter voltage on the Q25 until the voltage from the collector of Q24 to (-INP) on that inverter changes from 3 ± 1 volts to 19 ± 1 volts. The same voltage on the other inverter should reduce from 19 ± 1 volts to 3 ± 1 volts. There should be no further change when the separate power supply is disconnected from base to emitter of Q25.

2.9 Disconnect the voltmeters from the collector of Q24 and connect a dual channel oscilloscope to the collector of Q4 on both inverters. Set the oscilloscope on chopped, dual channel operation. Connect the common side of the oscilloscope to the (-INP) terminal. The collector of Q4 voltage on each inverter should be operating at the same frequency and in phase. Photograph the oscilloscope output to record this frequency locked condition.

3.0 Test of Phase Lock Circuits.

3.1 After completing Section 2.0, disconnect the oscilloscope from the collector of Q24 on each inverter. Connect the oscilloscope to the collector of transistor Q17A to (-INP) on each inverter. The voltage across each Q17A should be a square wave of the same frequency but not necessarily in phase with each other. Photograph the oscillograph picture to record the out-of-phase condition.

3.2 Close switch K4. This connects together the "H" terminals of both inverters and should lock both countdown circuits in phase with each other. The square wave voltages seen on the oscilloscope must now be in phase with each other. Photograph the oscilloscope picture to record the in-phase condition.

3.3 Disconnect the d-c power supplies.

4.0 Parallel Inverter Operation

4.1 Reconnect the inverter power stages to the d-c input which were disconnected in Section 2.2. Finish connecting the two inverters in parallel as shown in Figure 74.

4.1.1 Connect voltmeters, ammeters, wattmeters, and a frequency meter on each inverter output. Rated load current is 2.18 amperes.

4.1.2 Connect a separate 0-350 VA per phase, 0.9 leading to 0.75 lagging load to each inverter through a 3 PST switch.

4.1.3 Parallel the loads through an aircraft circuit breaker. Connect auxiliary contacts to short X1 to X2 on both inverters when the main contacts are open. This will disable the load division circuit during isolated operation.

4.1.4 Connect an ammeter and a voltmeter on each inverter input. Maximum d-c current is 50 amperes. Voltage varies from 26.0 to 30.0 volts d-c.

4.1.5 Open all switches and the paralleling circuit breaker.

4.2 Close switches K1, K2, and K3 to lock the frequency reference together.

4.3 Set loads at no load on each inverter. Close load switches to individual inverters but do not parallel the loads.

4.4 Connect one channel of a two channel oscilloscope to the collector of Q4 and (-INP) on inverter I. Connect the other channel to the collector of Q4 and (-INP) on inverter II.

4.5 Set both input d-c power supply voltages at 28 ± 2 volts and apply these voltages to the inverter.

4.6 When both Q4's operate at the same frequency, close switch K4 to lock the inverters in phase with each other.

4.7 Measure the voltage between V_{AI} and V_{AII}, V_{BI} and V_{BII}, V_{CI} and V_{CII}. These voltages must be 0 ± 2 volts. If they are not, adjust the appropriate R15. All line to neutral voltages on each inverter must be 115 ± 1 volt.

4.8 If the requirements of 4.7 are met, parallel the loads by closing the paralleling circuit breaker.

4.9 Operate the inverters in parallel and record the following data:

Load terminal voltages, 3Ø, L-N
Individual output currents
Individual output watts
Output frequency
Input voltage
Input current

4.9.1 Use the following loads:
0%
25%
50%
75%
100%
125%
at each of the following power factors:
.9 leading
1.0
.9 lagging
.75

NOTE: 100% load equals 250 VA per phase per inverter.

4.10 Repeat 4.3 through 4.8 except set the loads at those required in 4.9.1.

4.11 Using a recording oscillograph, record both phase A inverter output currents and voltages during the four 100% load paralleling transients required in section 4.10.

4.12 To demonstrate that an unloaded inverter can be paralleled with a loaded inverter, repeat 4.3 through 4.11 with one inverter unloaded and with the other inverter loaded to 100%, 1.0 PF. Record data called for in section 4.9 before and after paralleling. Use a recording oscillograph to record both phase A inverter output current and voltages during the paralleling transient.

4.13 To demonstrate that large load transients can be sustained by the paralleled inverters, parallel the unloaded inverters; then, simultaneously, apply two 100% 1.0 PF loads to the paralleled inverters. Record the data indicated in section 4.9 before and after applying the load. Use a recording oscillograph to record both phase A inverter output current and voltages during the application and removal of the load.

5.0 Single Converter Operation Test

5.1 Make terminal connections as shown in Figure 75. This connects the inverter output in delta and rectifies it through a three-phase full-wave rectifier. The output of the rectifier is connected to the + and - output terminals. Connect d-c output voltage, current, and wattmeters to these output terminals.

5.2 Connect a resistive load of 31.5 ohms (750 watt) across the output terminals.

5.3 Connect the d-c input source (E1) through a contactor to the input terminals. Set E1 at 28.0 ± 1.0 volts with the contactor open.

5.4 Close the input contactor.

5.5 Set the output voltage at 153.5 ± 1 volts d-c by adjusting potentiometer R15. Output current should be 4.88 amperes. Adjust load impedance, if necessary, to obtain this current.

5.6 Adjust the voltage across R69 to $20 \pm .1$ volts by adjusting R69. This adjustment establishes the transfer characteristics of the d-c current transducer in the d-c load division circuit so that one per unit load current (4.88 amps) is proportional to 20 volts between terminals Y1 and Y2.

5.7 Record the voltage across R69 for load currents from 0 to 6 amps by changing the load current in one ampere steps.

5.8 Repeat sections 5.0 through 5.7 for the second converter.

6.0 Parallel Converter Operation Test.

6.1 Connect two converters as shown in Figure 76.

6.1.1 Connect d-c voltmeters, ammeters, and wattmeters to each converter output. Rated current is 4.88 amperes d-c.

6.1.2 Connect a separate 0 to 1000 watt load to each converter through SPST switch.

6.1.3 Parallel the loads through an aircraft circuit breaker. Switch K6 is an auxiliary contact on this circuit breaker which closes when the main contacts are closed.

6.1.4 Connect a d-c voltmeter and ammeter to each converter input. Maximum d-c current is 50 amperes. Voltage varies between 26.0 and 30 volts d-c.

6.1.5 Open all switches and the paralleling circuit breaker.

6.2 Set both input d-c power supply voltages at 28 ± 2 volts d-c and apply these voltages to the converter input terminals.

6.3 Measure the voltage across the circuit breaker contacts. If this voltage is 0 ± 2 volt, close the circuit breaker.

6.4 Operate the converters in parallel and record the following data:

Output terminal voltage
Individual output currents
Individual output watts

6.4.1 Connect the following loads to each converter before closing the paralleling circuit breaker.

0%, 25%, 50%, 75%, 100%, 125%

NOTE: 100% load equals 750 watts/converter.

6.5 Using a recording oscillograph, record both converter output voltages and currents during the six paralleling transients of section 6.4.

6.6 To demonstrate that an unloaded converter can be paralleled with a loaded converter, parallel an unloaded converter with a converter loaded to 750 watts. Record data in accordance with section

6.4 before and after paralleling. Use a recording oscillograph to record both converter output currents and voltages during the paralleling transient.

6.7 To demonstrate that large load transients can be sustained by the paralleled converters, parallel the unloaded converters; then, simultaneously, apply two 750 watt loads to the paralleled converters. Record data in accordance with section 6.4 before and after applying the load. Use a recording oscillograph to record both converter output currents and voltage during the application and removal of the load.

7.0 Comparison Between Conventional Core Materials and "Cubex" Core Material in Output Transformer.

7.1 Connect one inverter as shown in Figure 73.

7.1.1 Connect input d-c voltmeter, ammeter, and wattmeter. Input voltage 26.0 to 30.0 volts. Maximum input current is 50 amperes.

7.1.2 Connect a complete set of three phase voltmeter, ammeters, and wattmeters. Rated output voltage is 115 volts rms line-to-neutral. Rated current is 2.18 amperes per phase.

7.1.3 Connect a 0 to 350 VA per phase, .9 leading to .75 lagging load to the output terminals.

7.1.4 Set d-c input voltage (E1) to 28 ± .1 volts d-c.

7.2 Perform sections 4.9 and 4.9.1 at 0 and 100% loads. Record transformer surface temperature.

7.3 Replace output transformer (P/N LYP18293D4) with Cubex-iron-core output transformer (P/N LYP18292D1).

7.4 Repeat paragraph 7.2 to determine differences in efficiency.

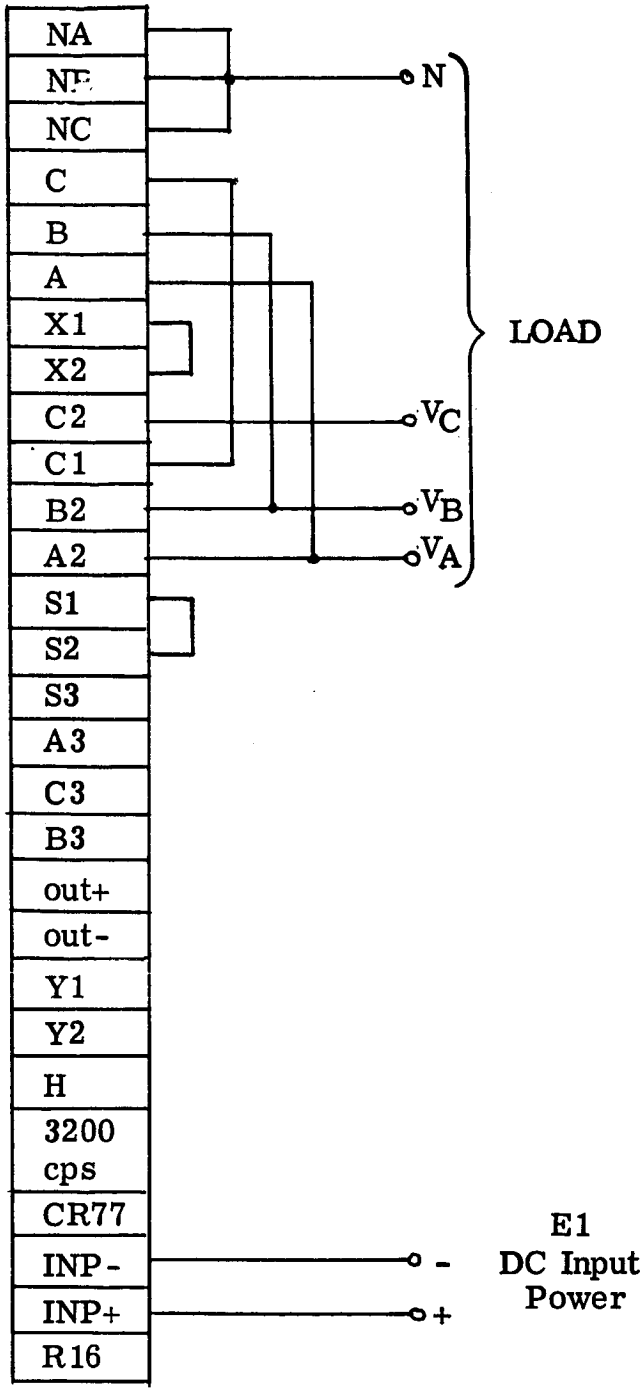


Figure 73. Terminal Connections for Single Inverter Operation and Initial Adjustments. (See Schematic Diagram.)

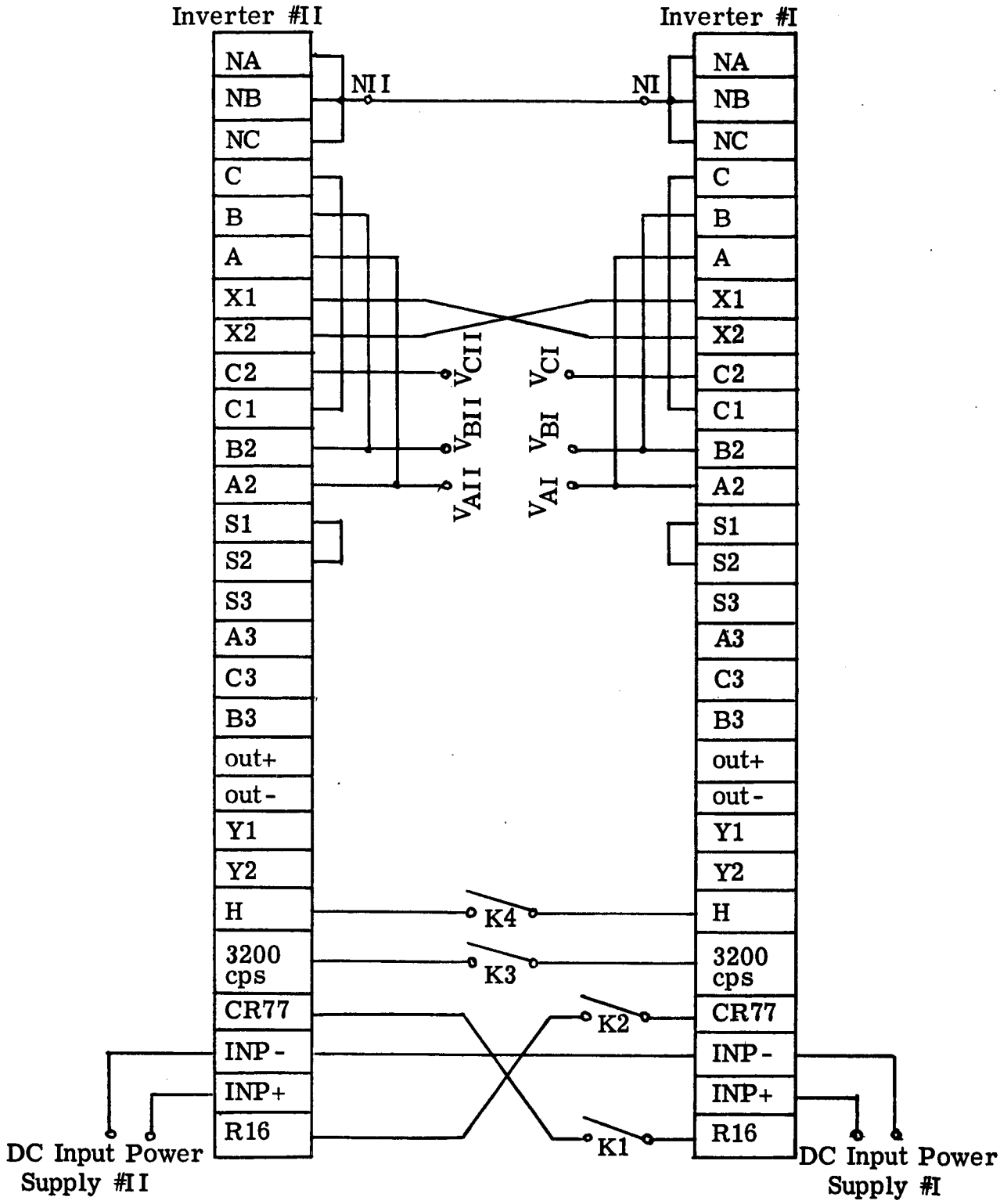


Figure 74. Terminal Connections and Interconnections for Parallel Inverter Operation. (See Schematic Diagram.)

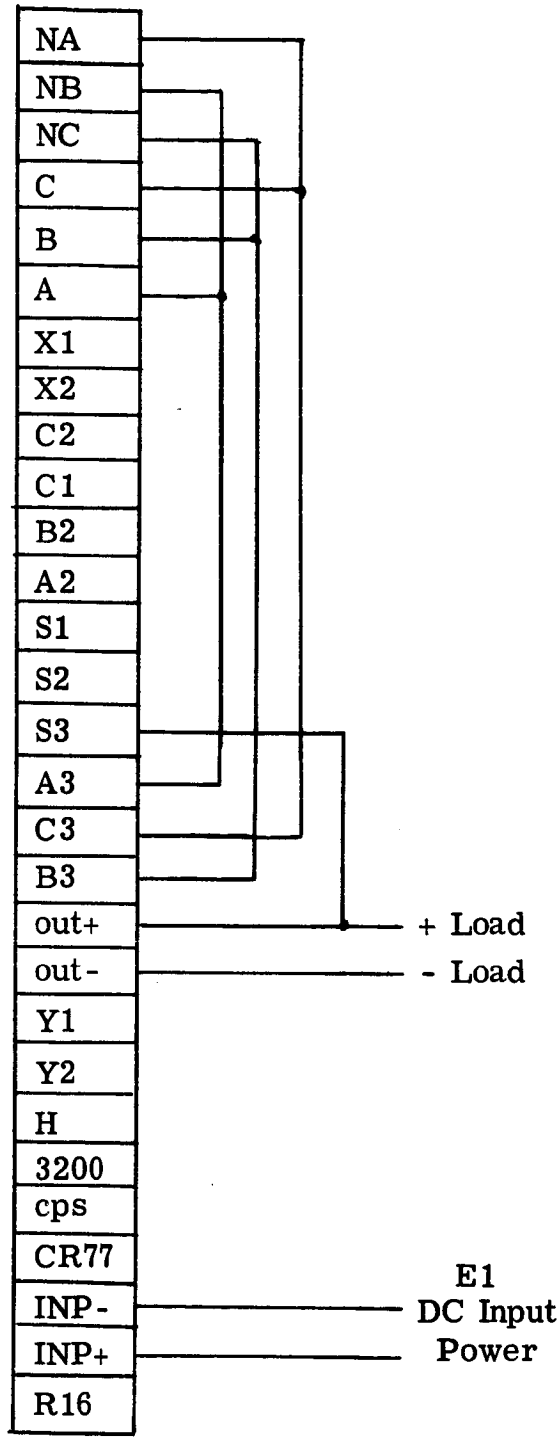


Figure 75. Terminal Connections for Single Converter Operation. (See Schematic Diagram.)

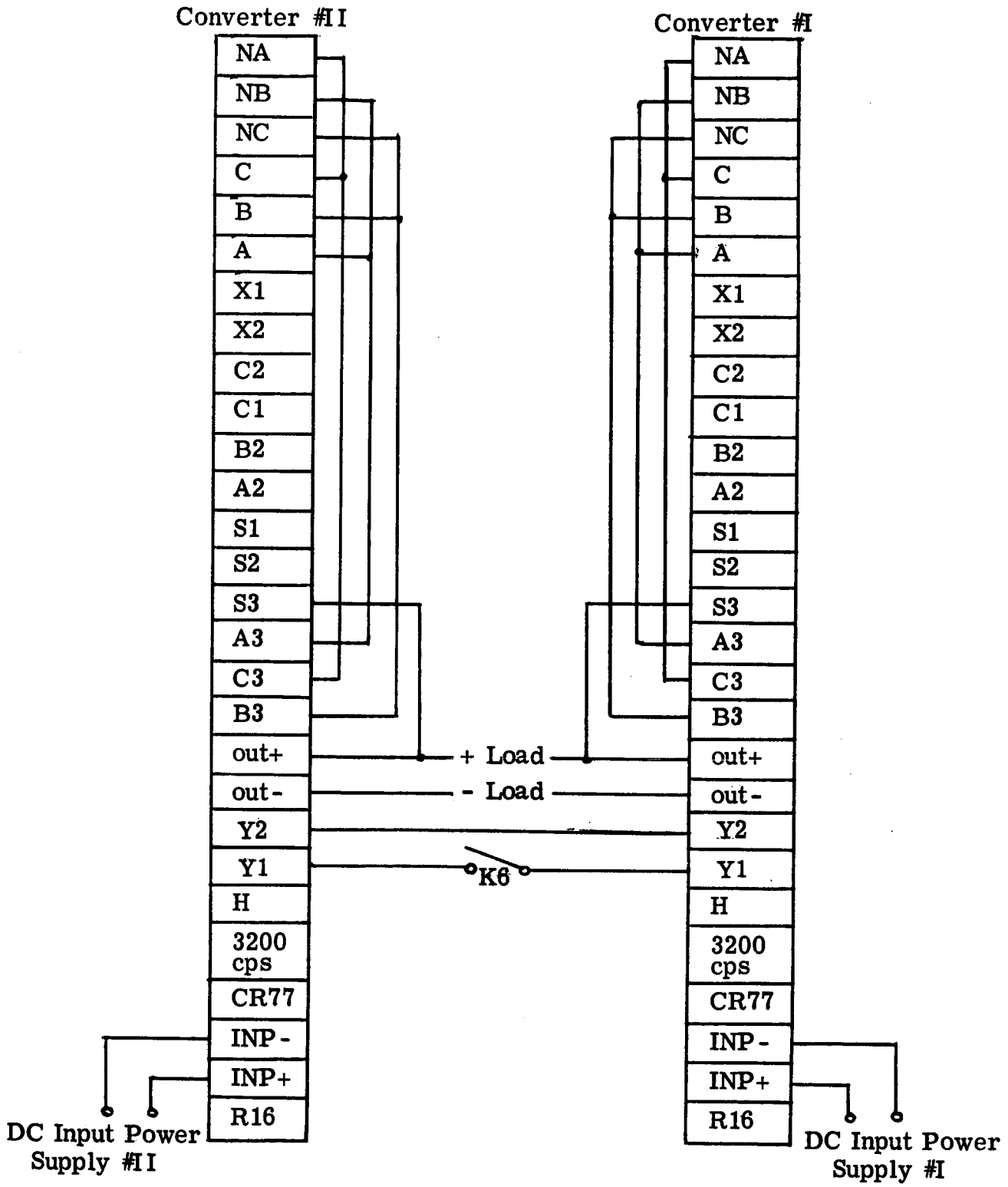


Figure 76. Terminal Connections and Interconnections for Parallel Converter Operation. (See Schematic Diagram.)

APPENDIX II

STATIC INVERTER INTERNAL IMPEDANCE MEASUREMENT

The most direct method of determining the internal impedance of a static inverter is by measuring the unregulated operating characteristics of the inverter under known load conditions. The internal impedance can then be easily calculated by one of two methods derived in this appendix. Both of these calculation methods consider that an unregulated static inverter can be considered as an a-c voltage source having a constant output voltage, $\dot{E}_1$, and an internal impedance, $\dot{Z}_1$ (a dot over a symbol denotes a phasor quantity). Figure 77 defines the symbols used in both derivations.

With the first method of calculating internal impedance, the inverter operating characteristics must be measured with no-load, a known load, and a three-phase short circuit. With the second method derived below, the inverter internal impedance can be calculated when the inverter operating characteristics have been measured at no-load and two other known loads.

Method 1 Derivation:

From Figure 77, the following relationship is evident:

$$\dot{E}_1 = \dot{Z}_1 \dot{I}_1 + \dot{V}_t .$$

We can select $\dot{Z}_L$. We can measure V_t and I_1.

Assume $\dot{V}_t = V_t \angle 0° ,$

$$\dot{Z}_1 = Z_1 \angle \theta_1 ,$$

$$\dot{Z}_L = Z_L \angle \gamma .$$

Therefore:

$$\dot{I}_1 = \frac{V_t \angle 0°}{Z_L \angle \gamma} = I_1 \angle -\gamma .$$

Fix

(1) $$\dot{E}_1 = \dot{V}_t \Big|_{\dot{Z}_L = \infty} = V_{toc} \angle \theta_o = \text{constant} \angle \theta_o$$

Then

$$V_{toc} \angle \theta_o = Z_1 I_1 \angle \theta_1 - \gamma + V_t$$

where θ_o, Z_1, and θ_1 are unknowns. We can derive two equations from equation (1) by separating the real and imaginary parts. Therefore, we need one more equation which relates the unknowns.

Thevinens equivalent circuit theory gives the needed relationship:

(2) $$Z_1 = \frac{E_{1oc}}{I_{1sc}}$$

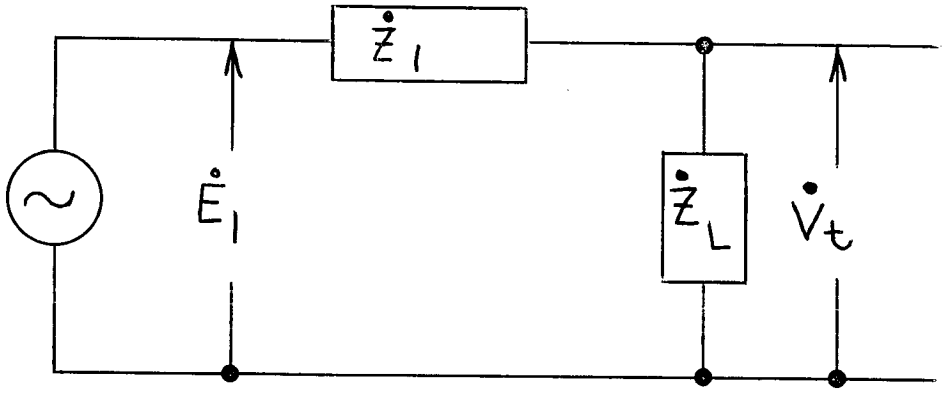


Figure 77. Equivalent Circuit of a Voltage Source

Where I_{1sc} is the rms phase current, I_1, with the three inverter output terminals short circuited, and E_{1oc} is the rms voltage V_t, with the three inverter output terminals open circuited. No change is allowed in the d-c voltage which is applied to the unregulated static inverter output stages when these quantities are measured. I_{1sc} should not exceed the rating of the inverter, so the d-c input voltage to the static inverter is reduced accordingly during these measurements.

Thus, equation (1) may be written as:

$$V_{toc}\angle\theta_o = \frac{E_{1oc}I_1}{I_{1sc}}\angle\theta_1 - \gamma + V_t .$$

By separating real and imaginary parts, the following two equations may be written:

$$(3) \quad V_{toc}\cos\theta_o = \frac{E_{1oc}I_1}{I_{1sc}}\cos(\theta_1-\gamma) + V_t ,$$

$$(4) \quad V_{toc}\sin\theta_o = \frac{E_{1oc}I_1}{I_{1sc}}\sin(\theta_1-\gamma) .$$

Square equations (3) and (4) and add the results:

$$(5) \quad V_{toc}^2 = \left(\frac{E_{1oc}I_1}{I_{1sc}}\right)^2 + \frac{2E_{1oc}I_1V_t}{I_{1sc}}\cos(\theta_1-\gamma) + V_t^2 .$$

Hence:

$$(6) \quad \cos(\theta_1-\gamma) = \frac{V_{toc}^2 - \left[V_t^2 + \left(\frac{E_{1oc}I_1}{I_{1sc}}\right)^2\right]}{\frac{E_{1oc}I_1V_t}{I_{1sc}}} .$$

Equation (2) can now be used to calculate the internal impedance magnitude, Z_1, and equation (6) can be used to calculate the angle, θ_1. The test measurements necessary to make these calculations can be made in the following manner:

I_{1sc} - Place a three phase short circuit across the inverter output terminals. Increase the d-c voltage to the unregulated power inverter stages until the short circuit output current, I_{1sc}, is at a reasonable magnitude (rated output current is reasonable).

E_{1oc} - Using the d-c voltage magnitude established above, remove the three phase short circuit from the inverter output and measure the inverter internal voltage, E_{1oc}, by measuring the open circuit inverter output voltage.

V_{toc} - Increase the d-c voltage to the unregulated power inverter stages until the open circuited output terminal voltage, V_{toc}, reaches a normal magnitude.

V_t, I_1, and γ - Without changing the d-c input voltage, apply a known load, $Z_L \angle \gamma$, and record the inverter output current, I_1, and terminal voltage, V_t. For most accurate results, the load should be near rated load. For resistive loads, $\gamma = 0°$. For other types of load, γ can be determined from the load power factor.

Method 2 Derivation:

A more general relationship can be derived if two different $\dot{Z}_L$'s are connected to the output terminals and the short circuit test is eliminated.

First assume:

$$\dot{Z}_{L1} = Z'_L \angle 0°,$$

$$\dot{I}_{11} = \dot{I}_1 \angle \gamma' = I_1 \angle 0°,$$

$$\dot{E}_{11} = V_{toc} \angle \theta'_0,$$

$$\dot{V}_{t1} = V'_t \angle 0°,$$

$$\dot{Z}_{11} = Z_1 \angle \theta_1.$$

so

$$(7) \quad V_{toc} \angle \theta'_0 = Z_1 I'_1 \angle \theta_1 + V'_t.$$

Then assume:

$$\dot{Z}_{L2} = Z''_L \angle \gamma''$$

$$\dot{I}_{12} = I_1 \angle -\gamma''$$

$$\dot{E}_{12} = V_{toc}\angle\theta_o''$$

$$\dot{V}_{t2} = V_t''\angle 0°$$

$$\dot{Z}_{12} = Z_1\angle\theta_1$$

so

(8) $$V_{toc}\angle\theta_o'' = Z_1 I_1 \cos(\theta_1 - \gamma'') + V_t''$$

Note: $\left|\dot{I}_{11}\right| = \left|\dot{I}_{12}\right| = I_1$. This condition has been made to simplify the following derivation. The condition can be easily met by properly selecting $\dot{Z}_{L1}$ & $\dot{Z}_{L2}$. Separate equation (7) into its real and imaginary parts:

(9) $$V_{toc}\cos\theta_o' = Z_1 I_1 \cos\theta_1 + V_t'.$$

(10) $$V_{toc}\sin\theta_o' = Z_1 I_1 \sin\theta_1.$$

Separate equation (8) similarily:

(11) $$V_{toc}\cos\theta_o'' = Z_1 I_1 \cos(\theta_1 - \gamma'') + V_t'',$$

(12) $$= Z_1 I_1 \cos\theta_1 \cos\gamma'' + Z_1 I_1 \sin\theta_1 \sin\gamma'' + V_t''.$$

(13) $$V_{toc}\sin\theta_o'' = Z_1 I_1 \sin(\theta_1 - \gamma''),$$

(14) $$= Z_1 I_1 \sin\theta_1 \cos\gamma'' - Z_1 I_1 \cos\theta_1 \sin\gamma''.$$

Solve equation (9) for $Z_1 I_1 \cos\theta_1$,

(15) $$Z_1 I_1 \cos\theta_1 = V_{toc}\cos\theta_o' - V_t'.$$

Substitute equations (10) and (15) in equations (12) and (14),

(16) $V_{toc} \cos \theta_o'' = (V_{toc} \cos \theta_o' - V_t') \cos \gamma'' + V_{toc} \sin \theta_o' \sin \gamma'' + V_t''$,

(17) $= V_{toc} \cos (\theta_o' - \gamma'') + V_t'' - V_t' \cos \gamma''$.

(18) $V_{toc} \sin \theta_o'' = V_{toc} \sin \theta_o' \cos \gamma'' - (V_{toc} \cos \theta_o' - V_t') \sin \gamma''$,

(19) $= V_{toc} \sin (\theta_o' - \gamma'') + V_t' \sin \gamma''$.

Square equations (17) and (19), and add the results:

(20) $V_{toc}^2 = V_{toc}^2 + 2V_{toc} (V_t'' - V_t' \cos \gamma'') \cos (\theta_o' - \gamma'') + 2V_{toc} V_t' \sin \gamma'' \sin (\theta_o' - \gamma'')$
$+ (V_t'' - V_t' \cos \gamma'')^2 + V_t'^2 \sin \gamma''$.

Expand $\cos (\theta_o' - \gamma'')$ and $\sin (\theta_o' - \gamma'')$ and collect terms,

(21) $2V_{toc} (V_t'' \cos \gamma'' - V_t') \cos \theta_o' = -2V_{toc} V_t'' \sin \gamma'' \sin \theta_o' - \left[(V_t'' \cos \gamma'' - V_t')^2 + V_t''^2 \sin^2 \gamma''\right]$.

Square both sides of equation (21):

(22) $4V_{toc}^2 (V_t'' \cos \gamma'' - V_t')^2 \cos^2 \theta_o' = 4V_{toc}^2 V_t''^2 \sin^2 \gamma'' \sin^2 \theta_o'$
$+ 4V_{toc} V_t'' \sin \gamma'' \left[(V_t'' \cos \gamma'' - V_t')^2 + V_t''^2 \sin^2 \gamma''\right] \sin^2 \theta_o' + \left[(V_t'' \cos \gamma'' - V_t')^2 + V_t''^2 \sin^2 \gamma''\right]^2$.

Substitute $\cos^2 \theta_o' = 1 - \sin^2 \theta_o'$ into equation (22) and collect terms,

(23) $4V_{toc}^2 \left[(V_t'' \cos \gamma'' - V_t')^2 + V_t''^2 \sin^2 \gamma''\right] \sin^2 \theta_o' + 4V_{toc} V_t'' \sin \gamma'' \left[(V_t'' \cos \gamma'' - V_t')^2 + V_t''^2 \sin^2 \gamma''\right] \sin \theta_o' + \left[(V_t'' \cos \gamma'' - V_t')^2 + V_t''^2 \sin^2 \gamma''\right]^2 - 4V_{toc}^2 (V_t'' \cos \gamma'' - V_t')^2 = 0$.

Divide equation (23) by

$$4V_{toc}^2\left[(V_t''\cos\gamma''-V_t')^2 + V_t''^2\sin^2\gamma''\right].$$

$$(24)\quad \sin^2\theta_o' + \frac{V_t''\sin\gamma''}{V_{toc}}\sin\theta_o' + \frac{\left[(V_t''\cos\gamma''-V_t')^2 + V_t''^2\sin^2\gamma''\right]^2 - 4V_{toc}^2\,(V_t''\cos\gamma''-V_t')^2}{4V_{toc}^2\left[(V_t''\cos\gamma''-V_t')^2 + V_t''^2\sin^2\gamma''\right]} = 0$$

So,

$$(25)\quad \sin\theta_o' = \frac{-V_t''\sin\gamma''}{2V_{toc}} \pm \frac{V''\cos\gamma''-V_t'}{2V_{toc}}\sqrt{\frac{4V_{toc}^2}{\left[(V_t''\cos\gamma''-V_t')^2 + V_t''\sin^2\gamma''\right]} - 1}$$

The value of $\sin\theta_o'$ must agree with equation (21). When the correct value of $\sin\theta_o'$ is determined, equations (9) and (10) are used to determine Z_1 and θ_1. Thus,

$$(26)\quad \tan\theta_1 = \frac{\sin\theta_o'}{\cos\theta_o' - \frac{V_t'}{V_{toc}}}$$

and

$$(27)\quad Z_1 = \frac{V_{toc}\sin\theta_o'}{I_1\sin\theta_1}$$

The test measurements necessary to calculate $Z_1\angle\theta_1$ using equations (25), (26) and (27) can be made in the following manner:

V_{toc} - Increase the d-c voltage to the unregulated power inverter stages until the open circuited output terminal voltage, V_{toc}, reaches a normal magnitude. This d-c voltage must be maintained throughout the following load measurements.

V_t' and I_1 - Apply a balanced three-phase resistive load to the unregulated static inverter and measure the terminal voltage, V_t', and load current, I_1. For most accurate results, I_1 should be close to the rated inverter output current.

V_t'' and γ'' - Maintain the same load current magnitude, I_1, while changing the power factor of the load $Z_L'' \angle \gamma''$. Record the new terminal voltage, V_t''. The angle, γ'', can be determined from the measured power factor of the load.

Measurement of The Internal Impedance of Static Inverter Model #2.

The procedure used to obtain experimental data to determine the internal impedance of static inverter model #2 is shown in Figure 78. See Figure 4 for terminal designations. Figure 79 contains the data obtained according to Figure 78. The following references to paragraphs are those paragraphs in Figures 78 and 79.

Example calculation of the internal impedance by method 1:

The data for paragraph 8 give :

$$I_{1sc} = \frac{2.18+2.14+2.28}{3} = 2.2 \text{ amperes.}$$

The data for paragraph 9 give :

$$E_{1oc} = \frac{35.8+36.1+36}{3} = 35.96 \text{ volts.}$$

The data for paragraph 4 give :

$$V_{toc} = \frac{115.8+115.0+114.8}{3} = 115.2 \text{ volts.}$$

The data for paragraph 5 give :

$$V_t = \frac{96.5+97.3+97.9}{3} = 97.23 \text{ volts,}$$

$$I_1 = \frac{2.18+2.18+2.16}{3} = 2.173 \text{ amperes,}$$

K 1565782

SUBJECT Inverter/Converter Model P/N LYP 18293 G1

CUSTOMER Engineering Dept. SERIAL NO. BB #2

S. O. OR TEST NO. N4-202 D. OR L. SPEC. NO. E2N-5J SHAFT NO. LYP18293 FRAME NO.

TO DETERMINE Inverter Internal Impedance

Procedure:

1. Disconnect the collectors of Q5 & Q6
2. Disconnect the gate signals to CR1 & CR2
3. Apply a stiff variable D.C. voltage source to + input & - C2. Call this voltage source E2
4. Operate power stage of inverter as usual at 400 CPS. Adjust E2 so that output voltage at A, B, & C equals 115 ± 1 volt. Record E2 and VAN, VBN & VCN.
5. Apply 2.18 ampere balanced resistive load to inverter output. Maintain E2 at same level as step 4. Record output volts, watts, and amps.
6. Apply 2.18 ampere balanced 0.75 P.F. lagging load to inverter output. Maintain E2 at same level as step 4. Record output volts, watts, and amps.
7. Repeat step 6 with 0.5 P.F. lagging load
8. Reduce E2 to zero. Place 3 ϕ short on inverter output. Increase E2 until output current equals 2.18 amps. Record E2 and output currents.
9. Remove three phase short. Maintain E2 same as in step 8. Record output voltages.

Continued on page K1565783

PREVIOUS TEST PAGE

Feb 26 1964 (DATE) W. Miller & D. Kidenour (SIGNED) G.W. Ernsberger (ENGINEER IN CHARGE)

Figure 78. Test Procedure Used to Determine the Actual Internal Impedance of the Inverter

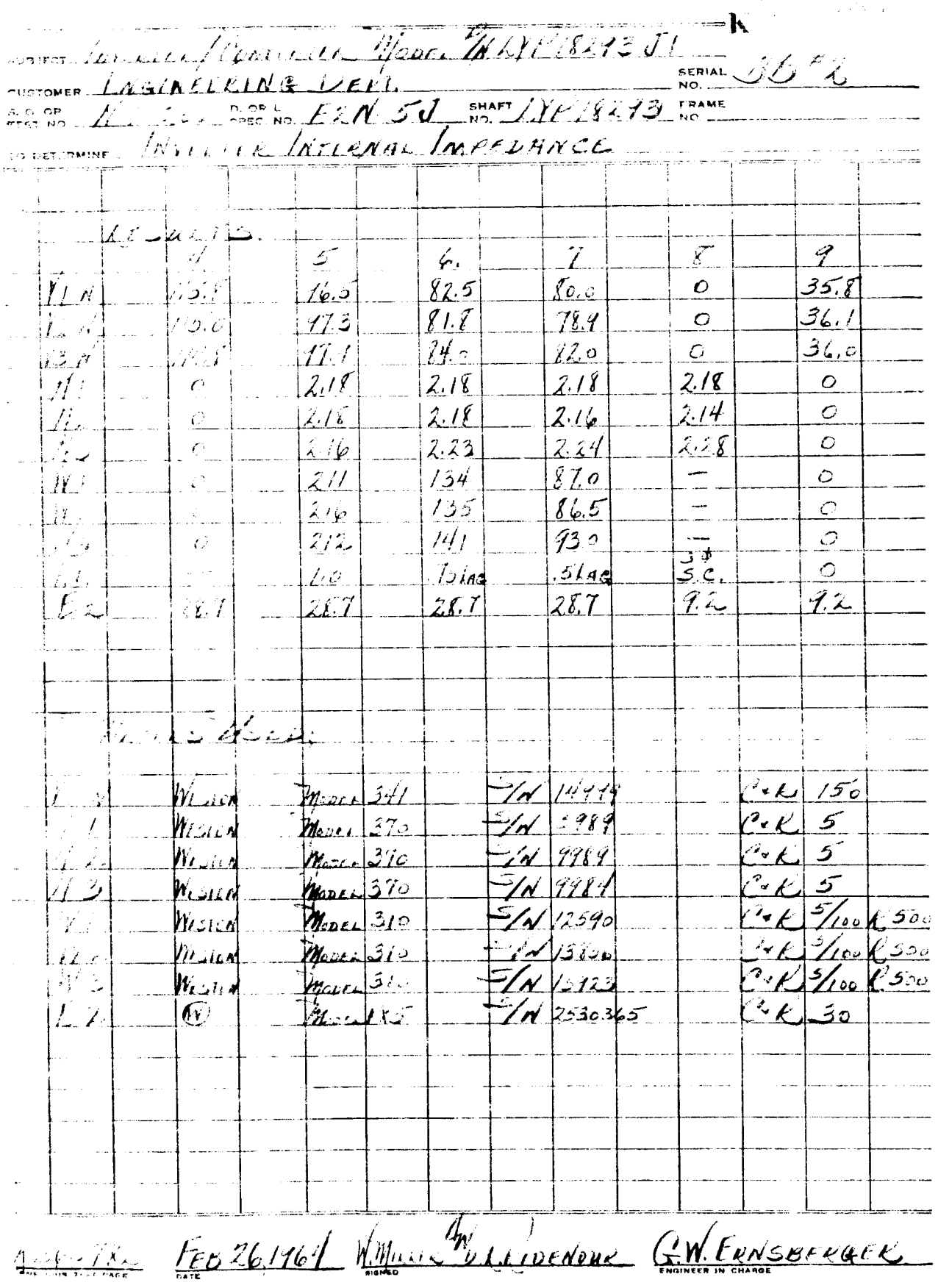


Figure 79. Data Taken to Determine the Actual Internal Impedance of the Inverter

$$\gamma = \cos^{-1} 1.0 = 0°.$$

Substitute these values into equation (6):

$$\cos(\theta_1 - 0) = \frac{(115.2)^2 - \left[(97.23)^2 + \left(\frac{35.96}{2.2}\,2.173\right)^2\right]}{\frac{2(35.96)(2.173)(97.23)}{2.2}},$$

$$\cos \theta_1 = 0.361;$$

or $\theta_1 = 68.8°$ as determined by method 1.

Substituting into equation (2) gives Z_1 by method 1:

$$Z_1 = \frac{35.96}{2.2} = 16.33 \text{ ohms.}$$

One per unit impedance is equal to the rated line voltage (115 volts) divided by the rated output phase current (2.18 amperes) or 53 ohms. Therefore, the static inverter internal impedance as determined by method 1 is:

$$\dot{Z}_1 = \frac{16.33}{53} \angle 68.8 = 0.308 \angle 68.8° \text{ P.U.}$$

Similar calculations using method 1 with the data of Paragraphs 6 and 7 respectively give:

with Para. 6 data:

$$\dot{Z}_1 = 0.308 \angle 71.4°$$

with Para. 7 data:

$$\dot{Z}_1 = 0.308 \angle 75°$$

These values compare very closely to the value derived in the first quarterly report of $0.27 \angle 77.8°$ P.U.

Example calculation of the internal impedance by method 2:

Using data from paragraphs 4, 5, and 6:

$$V_t' = 97.23 \text{ volts}$$

$$V_t'' = 82.76 \text{ volts}$$

$$\gamma'' = 41.4°$$

$$V_{toc} = 115.2$$

Using equation (25):

$$\sin\theta_o' = \frac{-(82.76)\sin 41.4°}{2(115.2)} \pm \frac{82.76\cos 41.4 - 97.23}{2(115.2)}\sqrt{\left[\frac{4(115.2)^2}{(82.76\cos 41.4 - 97.23)^2 + (82.76)^2\sin^2 41.4}\right]^{-1}}$$

$$= -0.237 \pm 0.522$$

$$= -0.759 \text{ or } +0.285$$

Thus:

$\theta_o = -49.4°$ or $16.6°$. One of these solutions is extraneous and must be eliminated by using equation (21).

Substitute $\theta_o' = 16.6°$ into equation (21):

$$-230.4(35.23)(\cos 16.6°) \stackrel{?}{=} 230.4(82.76)\sin 41.4)\sin 16.6° - (65.1)^2,$$

$$-7800 \stackrel{?}{=} -3610 - 4240,$$

$$-7800 \cong -7850.$$

Therefore $\theta_o' = 16.6°$ rather than $-49.4°$.

Using equation (26):

$$\tan \theta_1 = \frac{\sin 16.6^\circ}{\cos 16.6^\circ - \frac{97.23}{115.2}} = \frac{0.285}{0.958 - 0.844}$$

$$= 2.5;$$

$$\theta_1 = 68.2^\circ .$$

Using equation (27):

$$Z_1 = \frac{115.2 \sin 16.6}{2.2 \sin 82.8^\circ} = 16.1 \text{ ohms},$$

or $$Z_1 = \frac{16.1}{53} = 0.304 \text{ P.U.}$$

Therefore, $\dot{Z}_1 = 0.304 \angle 68.2^\circ$ P.U. as determined by method 2 and data from paragraphs 4, 5, and 6.

Using data from paragraphs 4, 5, and 7:

$$\theta_o' = 16.7^\circ$$

$$\dot{Z}_1 = 0.303 \angle 68.35^\circ \text{ P.U.}$$

The average of all five Z_1's calculated by both methods is:

$$\dot{Z}_1 = 0.305 \angle 70.3^\circ \text{ P.U.}$$

APPENDIX III

DERIVATION OF EQUATION (29)

Let R_I = reliability of an inverter

R_c = reliability of a changeover circuit

R_s = reliability of the system

n = number of inverters in the system

Item 1 is defined as a single inverter. Items 2 through n are each composed of an inverter and a changeover circuit.

The system fails only if all items fail.

A) Probability of failure of item 1 is $1-R_I$.

B) Probability of failure of item 2 is $1-R_IR_c$, by the product rule for series elements. The product rule is applicable because the failure of item 2 may be caused by the failure of either of its elements.

C) The probability of failure of item 3, 4, 5, etc. is the same as item 2, because they are identical.

The probability of system failure is the probability of the failure of all items, and is by the product rule $(1-R_I)(1-R_IR_c)^{n-1}$.

System reliability = 1 - probability of system failure

$$(29) \quad R_s = 1 - (1-R_I)(1-R_IR_c)^{n-1}$$

APPENDIX IV

ANNEALING OF HIPERSIL AND CUBEX STEEL TRANSFORMER LAMINATIONS

The Hipersil steel transformer laminations were punched from 0.011 inch thick Hipersil steel sheet obtained from the Westinghouse Transformer Division, Sharon, Pennsylvania. (This material is also available from Armco Steel Corporation, Middletown, Ohio.) These punchings were annealed in a dry hydrogen atmosphere (dew point did not exceed -20°C) at 800°C ± 10°C for two hours and then furnace cooled to below 150°C.

The CUBEX steel transformer laminations were punched from 0.006 inch thick sheet obtained from the Westinghouse Research & Development Center, Pittsburgh 35, Pennsylvania. To provide the means to establish a magnetic field in the laminations during the annealing process, a fixture was constructed and is shown in Figure 80. The four plates shown were made from 3/8 inch thick Inconel. The two coils were wound from 1/4 inch O.D. low-oxygen copper rod. The rod was flame sprayed with alumina to insulate the conductors during the anneal.

Sufficient CUBEX steel laminations were punched for two transformers so that two separate anneals could be made. Half of the laminations were assembled into the annealing fixture. A Westinghouse Type HS-12 furnace was pre-heated to 1000°C. The assembled fixture was placed in an enclosed Inconel retort. The cold retort was inserted into the furnace and raised to 900°C. The charge was maintained at 900°C for ninety minutes. A 10 oersted field was then applied and held during the entire cooling cycle. During the entire anneal, a dry hydrogen atmosphere was present. A flow rate of 30 cubic feet per hour was accurately metered and dew points were checked at the beginning, mid-point, and end of the cycle. The entrance dew point was greater than -65°C. The exit dew points were not less than -35°C. The cooling cycle for the first anneal was programmed at 2°C per hour. The cooling cycle for the second anneal was programmed at 25°C per hour. Magnetic tests conducted after the two anneals showed that the magnetic properties were not changed by cooling rate.

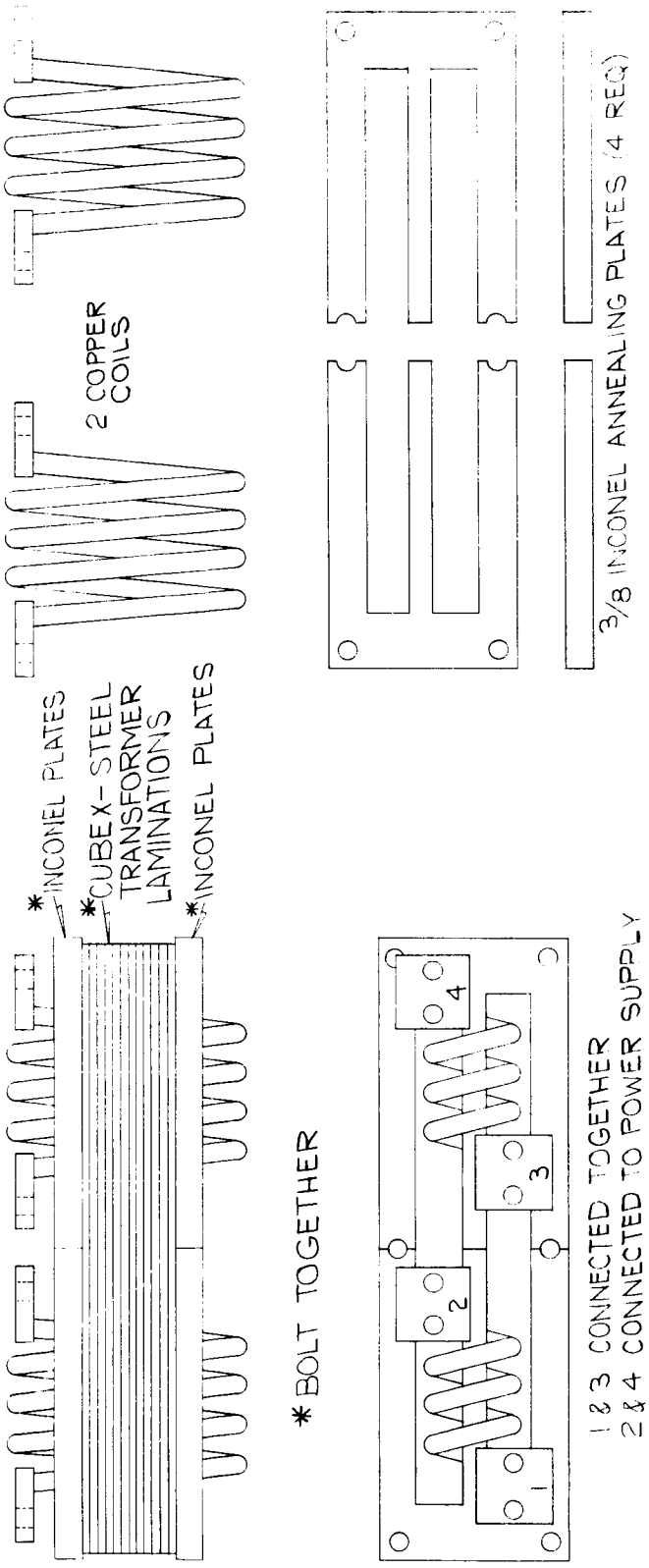


Figure 80. Fixture Used to Establish a Magnetic Field in the CUBEX Steel Transformer Laminations During the Annealing Process

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